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Electrostatic and Dynamic Analysis of P+PNP Double Junction Type and P+PNPN Triple Junction Type Pinned Photodiodes

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Abstract: This paper explains the device structure and operation of image sensors and solar cells. Both are semiconductor devices operating with the same physical principle of detecting photons. A high efficiency of the photon to electron energy conversion is very much desired in both devices. Image sensors now use a very advanced and scaled down CMOS fabrication process technology to achieve high performance features such as the excellent short wave blue light sensitivity for good color reproduction, the low noise and the no image lag picture quality for filmless and mechanical free action cameras. On the other hand, solar cells are still now built with the primitive floating N+P single junction type photodiode to minimize the fabrication process cost but with very low energy conversion efficiency of about 20%. It is explained in details that the depletion region of the PN junction is not the only place where we can achieve photo electron and hole pair separations effectively. The short-wave blue light has only 1000 Å silicon crystal penetration depth. The pinned surface P+P Gaussian doping profile has a very important role to achieve a better photon to energy conversion efficiency, especially for the short-wave blue light. Electrostatic and dynamic behaviors of Pinned Surface P+PNP Double Junction type Dynamic Photo Transistor and Pinned Surface P+PNPN Triple Junction type Dynamic Photo Thyristor are analyzed in details. Both of them are shown to be expected to have much excellent photon-to-electron energy conversion efficiency.

Keywords: Pinned Buried Photodiode, Double Junction Dynamic Photo Transistor, Triple Junction Dynamic Photo Thyristor, Empty Potential Well, Rotary Shutter, Global Shutter, Surface Barrier Potential, Double Junction Type Solar Cell

1. Introduction

The human eye balls convert the light energy to the electron energy. The in-coming light thru the iris excites the retinal cells inside a human eye ball. The retinal cells convert the light signal information into the corresponding electrical signals.

Subsequently, a long line of nerve cells transfers the electron signal charge to the receiving human brain. Being stored in the form of an excited photo electron energy, the input signal is further processed and the output results of the processed information are stored in the human brain. The long line of nerve cells acts as a Charge Transfer Device (CTD) while the human brain acts as a central processing unit (CPU) and an information memory storage. A typical image sensor is composed of three parts likewise. They are (1) the photo detecting device (PPD) like the retina cells, (2) the Charge Transfer Device (CTD) like the long line of nerve cells and (3) the signal processing CPU and Memory Units like the human brain. See Figure 1. In a typical classical MOS type CTD image sensor the first part is a single N+P floating diffusion junction type dynamic photo capacitor type PPD. The second part is a CTD with an analog signal data output line which is very similar in organization with the simple 1T1C DRAM digital signal data output line. And the third one is a single metal oxide semiconductor (MOS) transistor type source follower current amplifier circuit. The short-wave blue light has only 1000 Å silicon crystal penetration depth and cannot penetrate the thick N+ floating-surface diffusion region. Figure 2 compares the single N+P floating diffusion junction type PPD and the double P+PNPP+ junction type PPD.

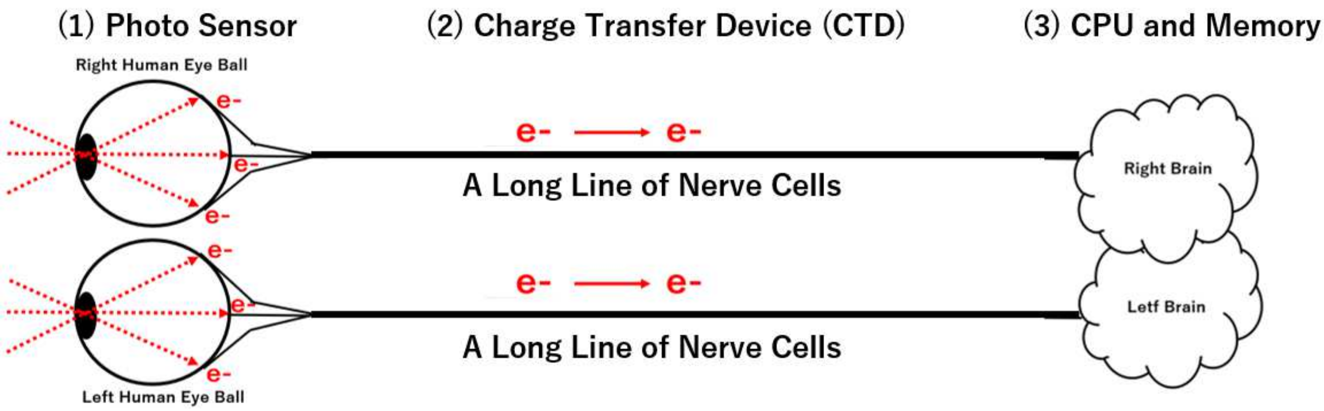


Figure 1. *Artificial Intelligent (AI) Image Sensor Structure with Three Basic Parts.*

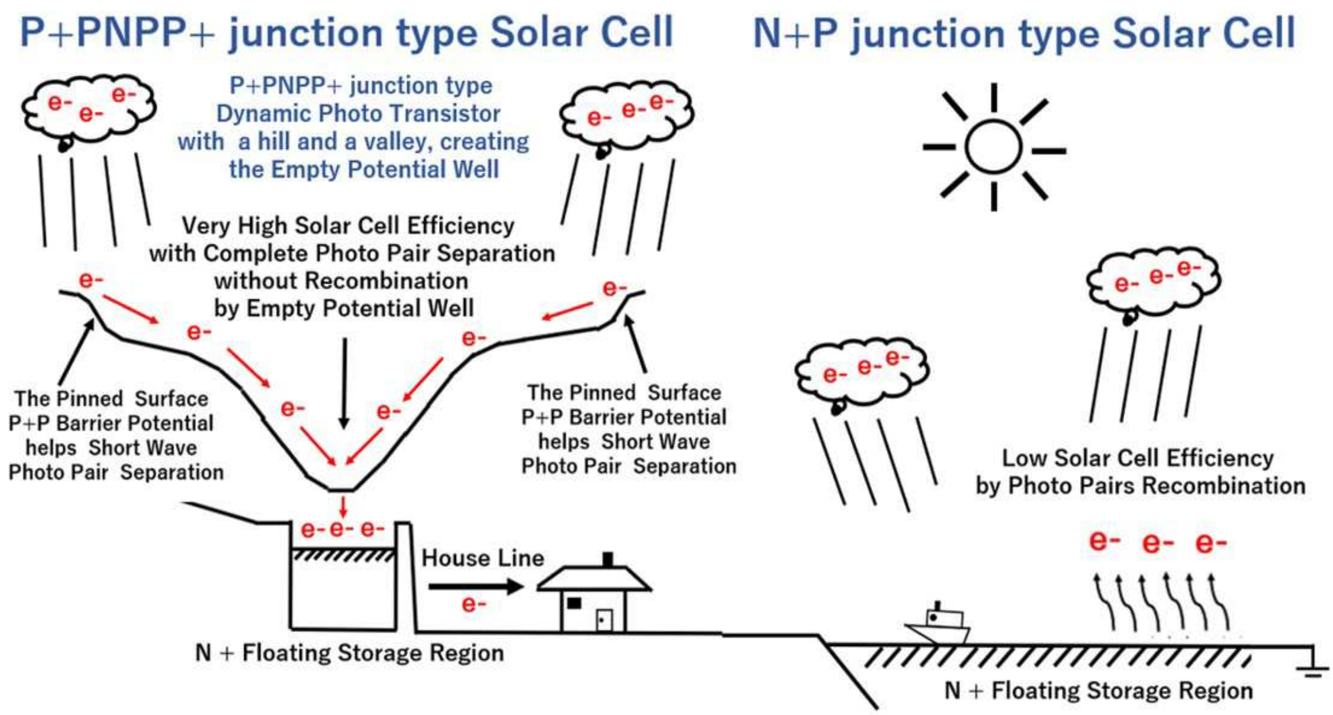


Figure 2. *Comparison of Double and Triple Junction type Photo Sensor Structures.*

2. Problems of Classical N+P Single Junction Photodiode and CCD/MOS Photo Capacitor Type Photo Sensor

As shown Figure 3, a classical MOS image sensor had a large output-data-line clock noise and a serious CkT noise [1]. In 1970 the CCD/MOS dynamic photo capacitor type PDD and CTD were invented by Boyle and Smith in Bell Lab [2-3]. The image sensors using the CCD type CTD were prevailing in 1980s and 1990s. Specially the Buried Channel CCD type PPD and CTD have the charge transfer efficiency of about 99.999%, which was enough in the analog TV era for the picture size of 800H x 500V pixels. However, presently CMOS image sensors have replaced CCD image sensors completely in the image sensor market. In the high-definition picture size of 8000H x 6000H pixels and more, we now need to have at least 8000+6000=24000 times of the charge transfer operation in case of the CCD type charge transfer device (CTD). Since 0.001% times 24000 gives 24%, the significant percentage (24%) of the signal charge is lost as the signal noise in the CCD type CTD image sensor. The Buried Channel CCD charge transfer efficiency of about 99.999% is now no longer enough in the high-definition digital TV era. Moreover CCD/MOS type dynamic photo capacitors need the metal like polysilicon electrodes which do not pass the short-wave blue light. Historically, Sony once used in 1980 the thin polysilicon electrode type CCD/MOS dynamic photo capacitors for the Interline Transfer (ILT) CCD type CTD image sensors [4]. See Figure 4. But the surface electric field under the CCD/MOS electrode induced serious surface dark current and generated many white defects in the re-produced picture images, causing serious yield problems in mass production.

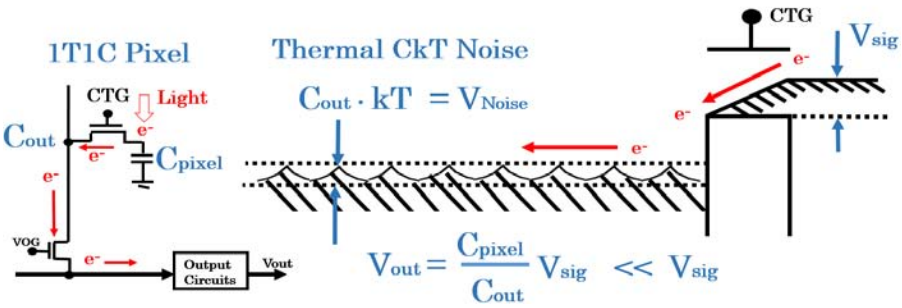


Figure 3. *1T1C type MOS Image Sensor with a Large Output Data Line Capacitance.*

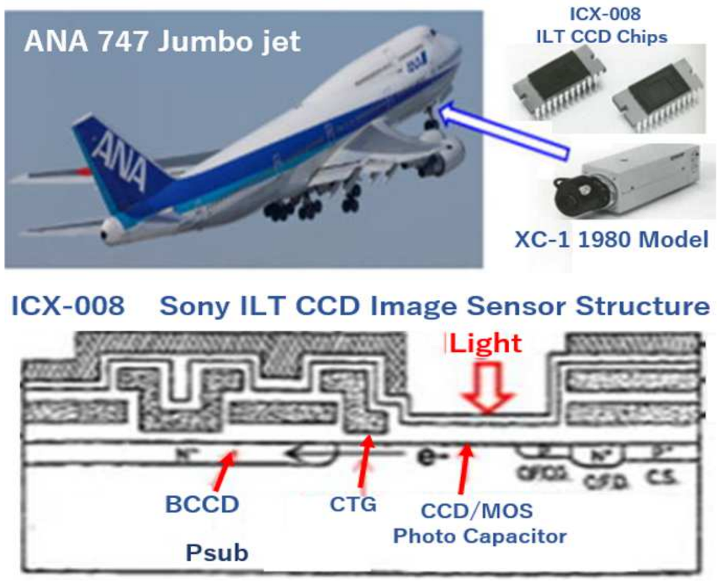


Figure 4. *SONY 1980 Two-chip CCD Color Video Camera XC-1.*

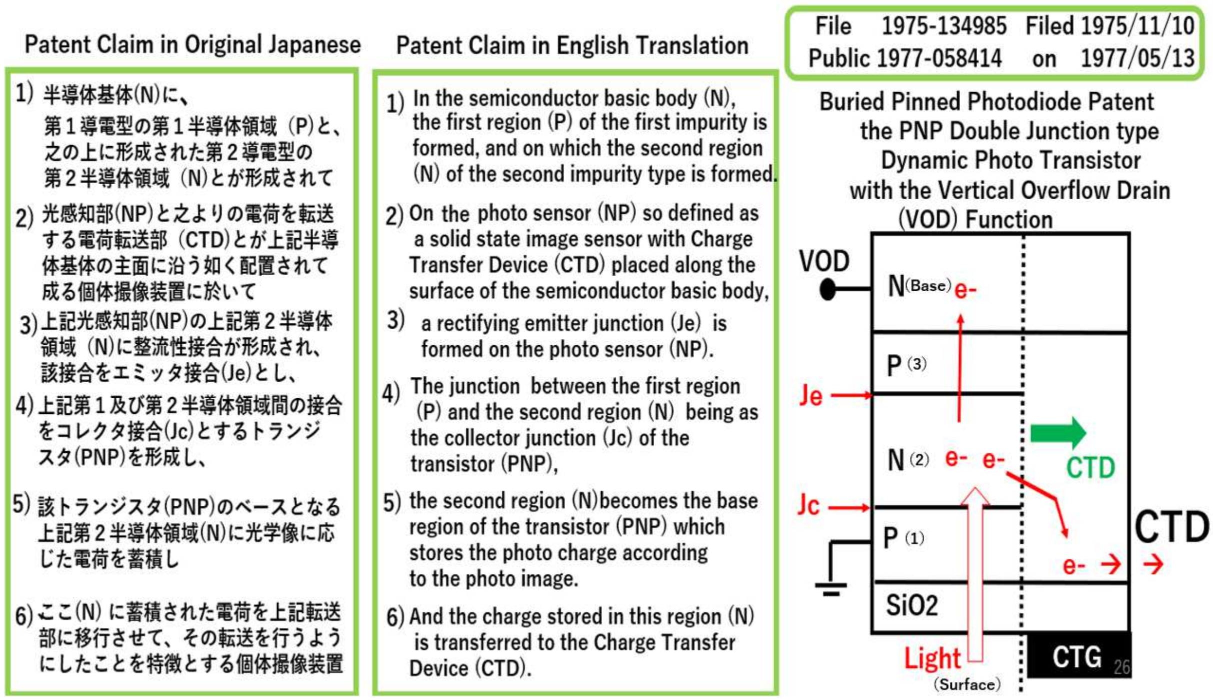
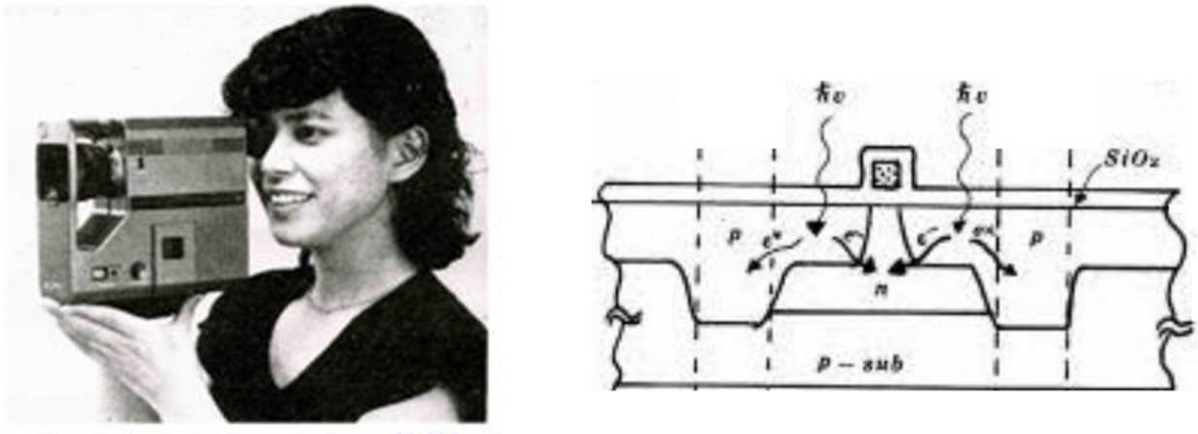


Figure 5. *Patent Claim of JPA1975-134985 on the PNPN Dynamic Photo Thyristor with Pinned P+ surface (HAD).*

3. Invention of P+NPN Triple Junction Dynamic Photo Thyristor Type Pinned Photodiode by Hagiwara in 1975

A new double junction type dynamic photo transistor and triple junction type dynamic photo thyristor were invented by Yoshiaki Hagiwara at Sony in 1975 [5]. See Figure 5. The PNPN thyristor has the punch-thru operation mode that had a potential application for the image lag free electric shutter function. Hagiwara team in Sony subsequently developed PNP double junction type photo sensors in 1978 and reported in details in the SSDM1978 conference in Tokyo, Japan [6-7].

Figure 6 shows a proto type of one chip video camera with the VTR 8mm tape. Sony focused in producing the image sensor products. It took more than ten years for Sony to develop the ILT CCD type image sensor with the PNPN triple junction type dynamic photo thyristor with the completely mechanical-part free electrical shutter function and completely image lag free feature [8]. Sony named this triple junction type dynamic photo thyristor type sensor structure with the P+ pinned surface as Hole Accumulation Diode (HAD). Sony introduced in 1987 the passport size compact video camera using this Pinned Photodiode which was originally invented by Yoshiaki Hagiwara at Sony in 1975.



Sony 1980 Video Movie has in one body an 8 mm VTR and One Chip FT CCD Image Sensor with the PNP Double Junction type Pinned Photodiode developed by Hagiwara in 1978

PNP Double Junction Pinned Photodiode with Heavily Doped P+ Adjacent Channel Stops reported in SSDM1978 by Hagiwara at Sony

Figure 6. *SONY 1980 Video Movie with the PNP Pinned Photodiode by the adjacent P+ channel stops.*

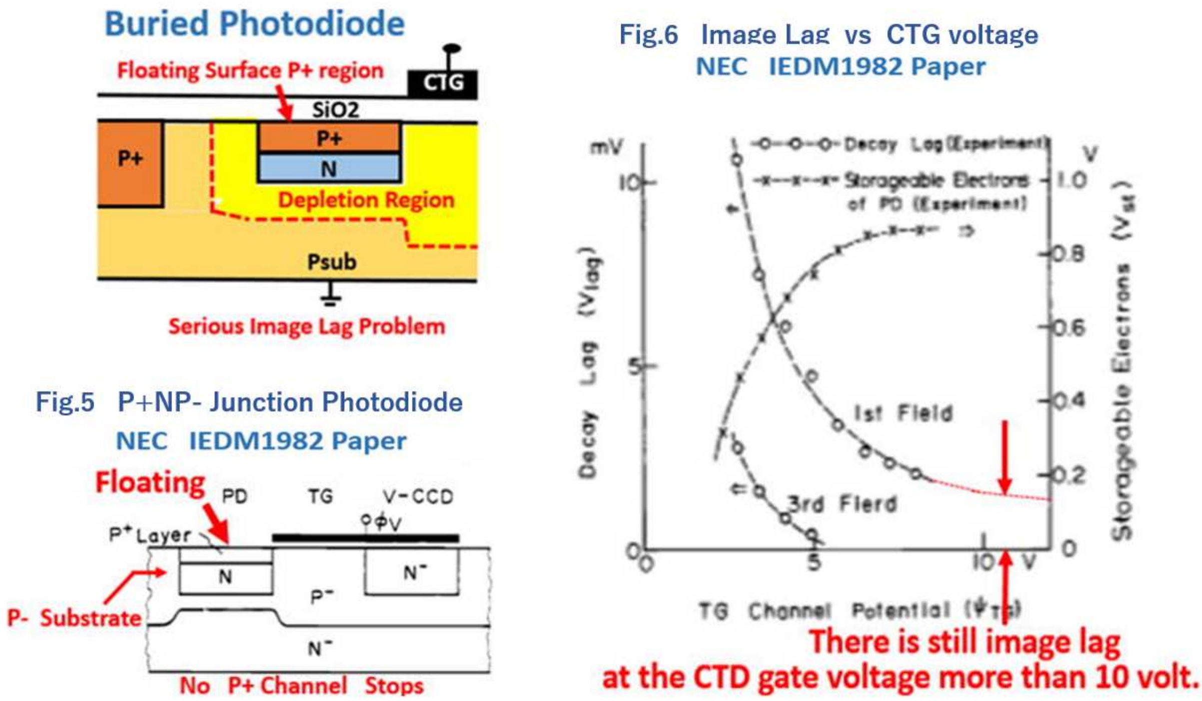


Figure 7. *The Buried Photodiode with the Image lag problem reported in NEC 1982 IEDM paper.*

4. Difference of Buried Photodiode and Pinned Photodiode

Sony focused in producing the image sensor products and kept silent till 1987 for business purpose. Meanwhile in 1982 NEC reported the same double junction type PNP photodiode in the IEDM1982 conference and named it as Buried Photodiode (BPD). NEC reported the details of the image lag problems of the Buried Photodiode [9-10]. See Figure 7. The depletion region of a PN junction acts as a capacitor element isolating the both terminals of the P and N regions. Hence the P and N regions can have different voltage levels. Similarly, by the two-dimensional electro dynamic effect, the simple P+PP+ structure can act as a capacitor element when the center P region is completely depleted. The completely depleted central P region can also isolate electrically both terminals of the left and right P+ regions. See Figure 8 for the surface potential profiles VS(x). Apparently, no adjacent P+ heavily doped channel stops region was not shown in the NEC photodiode. And consequently, it can be concluded that NEC photodiode has a floating surface P+ hole accumulation region. This is a floating N buried storage region which is similar to the classical simple floating surface N+ region of the N+P single junction photodiode with the serious image lag. This is why NEC reported the serious image lag problems in the IEDM1982 paper. Pinned Photodiode is always Buried Photodiode but Buried Photodiode is not always Pinned Photodiode.

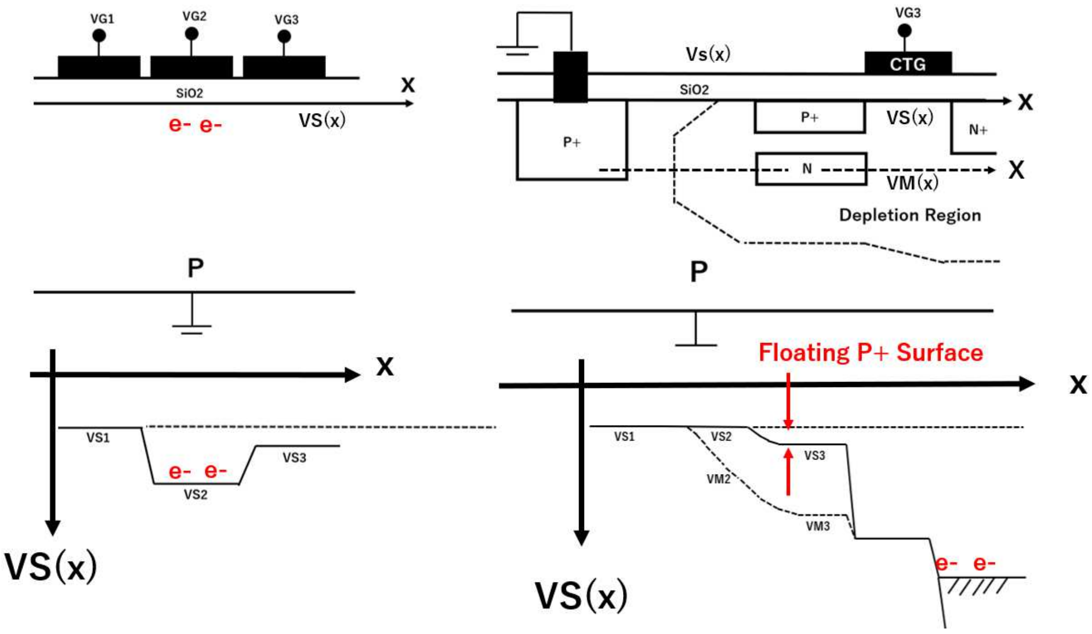


Figure 8. The Buried Photodiode with the Image lag problem reported in NEC 1982 IEDM paper.

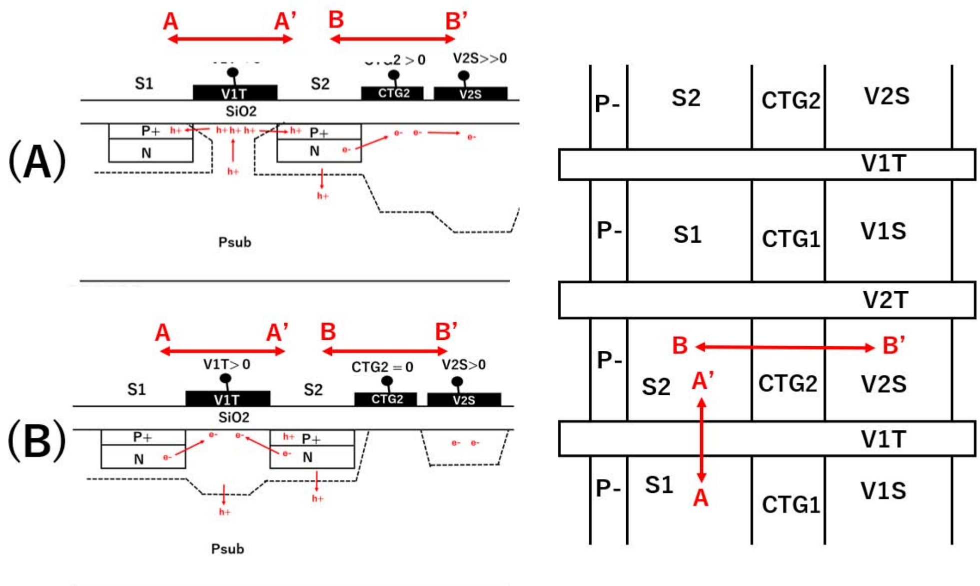


Figure 9. The problems of the ILT CCD Image Sensor without P+ Channel Stops Region.

Figure 9 shows the problems of the Interline Transfer CCD image sensor without the adjacent heavily doped P+ channel stops region. If the device isolation region has a thin oxide under the metal electrode, the negative voltage swing of the metal wire influences the semiconductor surface. And the surface will become the state of hole accumulation and pinned to the ground voltage by the holes entering from the grounded substrate. The depletion surrounding the floating P+ surface region over the buried N charge storage region will be diminish and the holes can enter the P+ surface region. Consequently, the floating P+ region will be pinned and grounded by the holes entering from the P- lightly doped P-type substate.

On the other hand, when the positive gate voltage swing is applied to the metal wire over the device isolation region, if the oxide under the metal wire is thin, the surface under the metal wire will be inverted and the surface potential under the metal wire of the device isolation region will become deep with a high positive electron potential. The photo electrons stored in the buried N storage regions will be attracted to the inverted surface region of the device isolation and photo signal electrons are mixed. The device isolation regions do not function as expected any longer. Figure 10 explains the effect of the capacitor couplings induced by the depletion region extended from the positive voltage of the buried N photo signal charge storage region. In conclusion, without the adjacent P+ heavily doped channel stops, the P+PN double junction buried photodiode never becomes Pinned Photodiode.

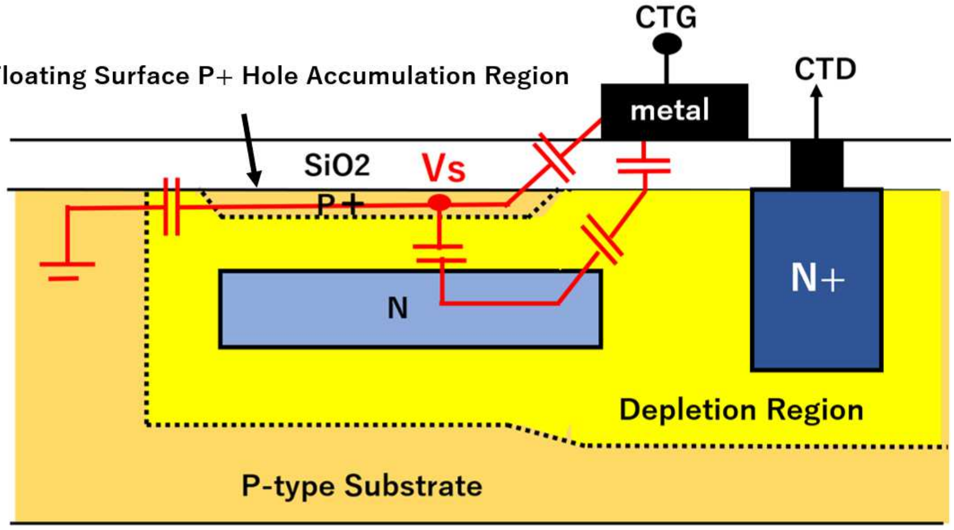


Figure 10. *Capacitor Couplings of the Floating Surface P+ Hole Accumulation Region.*

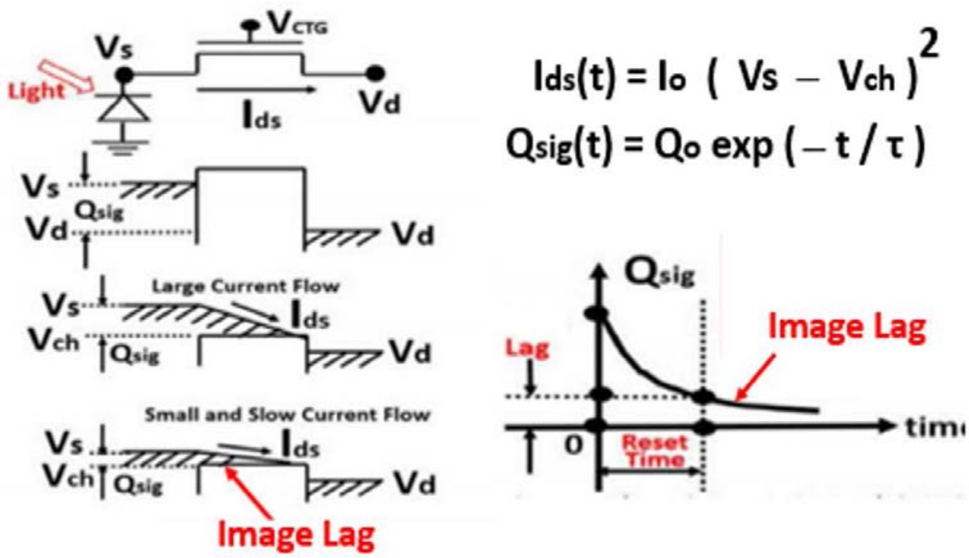


Figure 11. *Serious Image Lag of Floating N+P Single Junction Photodiode.*

Figure 11 explains how the floating surface causes the serious image lag problem. Subsequently KODAK in the IEDM1984 conference reported the details of the excellent feature of the low surface dark current of the pinned surface PNP double junction type Pinned Photodiode. KODAK IEDM1984 paper emphasized the importance of the heavily doped surface P+ must be pinned externally directly connected to the substrate ground voltage by the adjacent heavily doped P+ channel stops regions. KODAK named this photodiode with the Pinned P+ surface region as Pinned Photodiode [11]. However, in the Japanese patent application, JPA1975-127647, in 1975, Hagiwara at Sony invented the N+NP+N double junction type Pinned Photodiode structure with the pinned N+ surface and the empty potential well of the complete charge transfer with no image lag problem [12].

The surface potential is flat with no surface electric field that induces the undesired surface dark current. See Figure 12. Besides the three-level clocking scheme and the CCD/MOS dynamic capacitor memory for signal charge storage, as shown in the patent figure of JPA1975-127647, can be used for the built-in Global Shutter function, which is very essential and needed for modern CMOS image sensors to suppress the undesired rotary shutter effect. Both NEC IEDM1982 paper and KODAK IEDM1984 paper failed to quote as the reference the original Japanese patent inventions of the double junction type dynamic photo transistor and triple junction type dynamic photo thyristor proposed by Yoshiaki Hagiwara at Sony in 1975 and the detailed presentations reported by Hagiwara at the SSDM1978 conference in Tokyo, Japan.

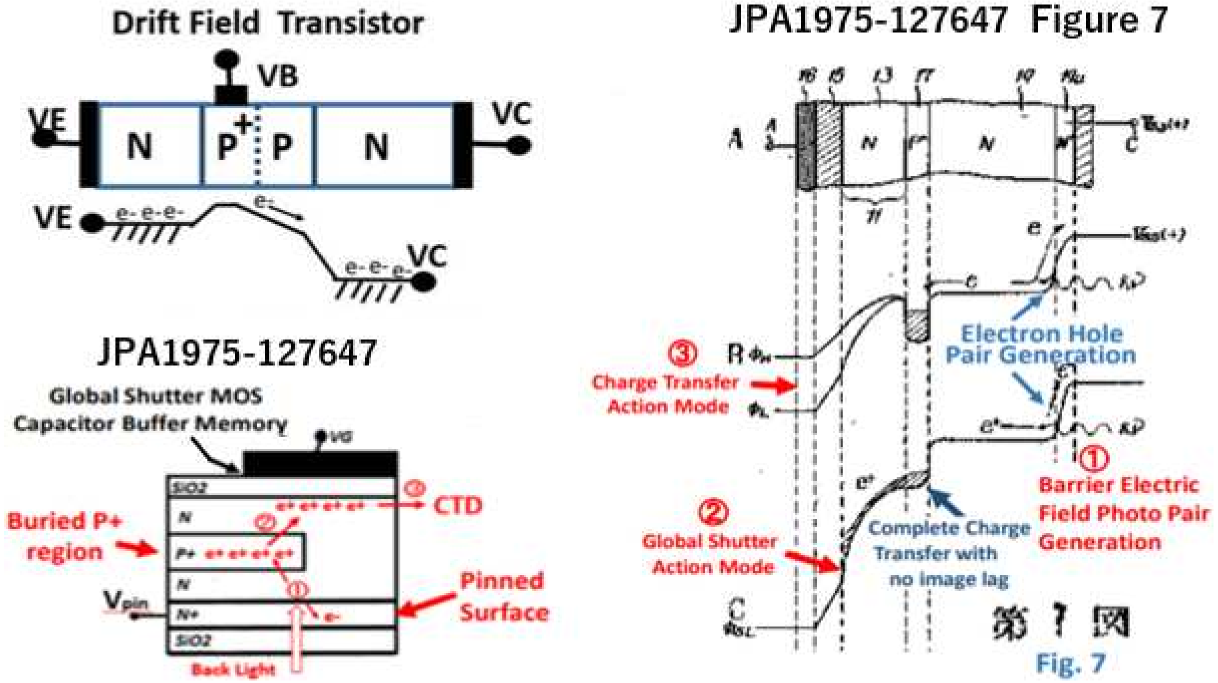


Figure 12. *The N+NP+N type Pinned Photodiode defined in Figure 7 of JPA1975-127647 patent by Hagiwara.*

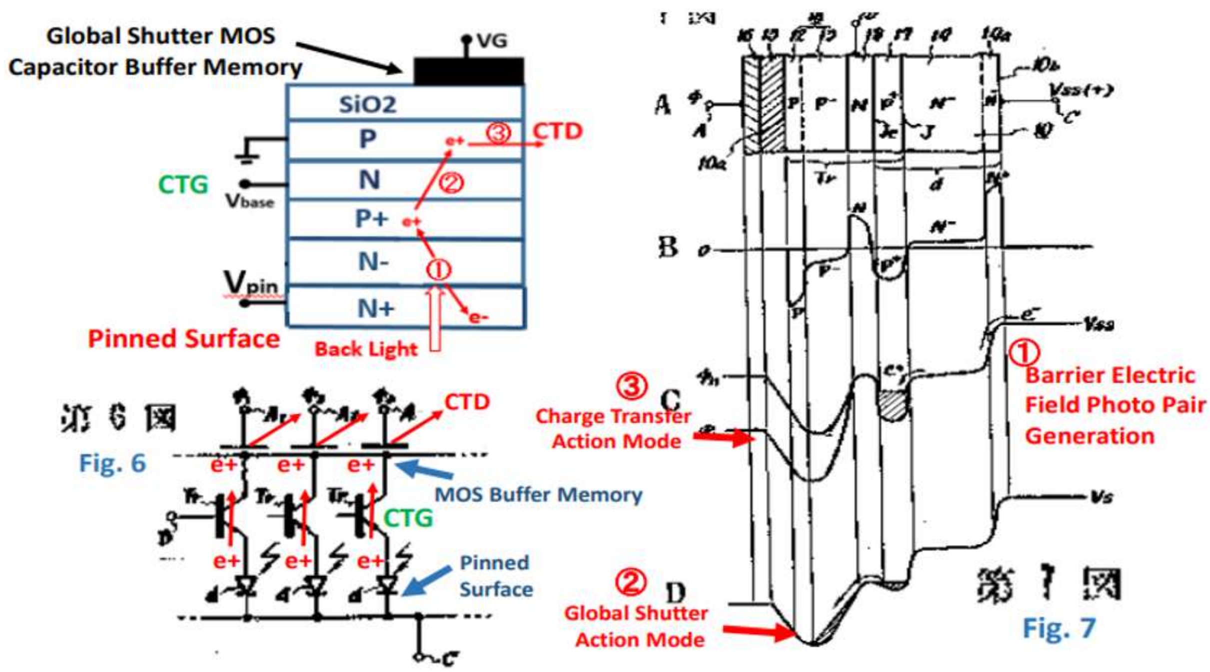


Figure 13. *The N+NP+N type Pinned Photodiode defined in JPA1975-127647 patent by Hagiwara.*

The problem was that the four basic 1975 Japanese Patent Applications, (1) JPA1975-134985 shown in Figure 5, (2) JPA1975-127647 shown in Figure 10, (3) JPA1975-127646 shown in Figure 13 which describes the pinned and buried N+N-P+NP triple junction type dynamic photo thyristor with the base punch-thru operation mode of the PNP bipolar transistor gating structure and (4) JPA1977-126885 shown in Figure 14 which describes the electric shutter function scheme and the gamma control scheme proposed by Hagiwara in 1977, were all applied only in Japanese patent office and, besides all being written in Japanese, were very hard to be accessed and also were never disclosed in the English-speaking community. Although Hagiwara SSDM1978 paper on the pinned-surface PNP double junction type pinned and buried photodiode was written and reported in English, the SSDM1978 conference had a limited number of attendants. Besides, the SSDM1978 conference technical journal was not well circulated. For this reason, in this paper now explained are the details and future potential applications of the P+P pinned-surface and buried photodiodes with the N-type photo-charge storage [13-14].

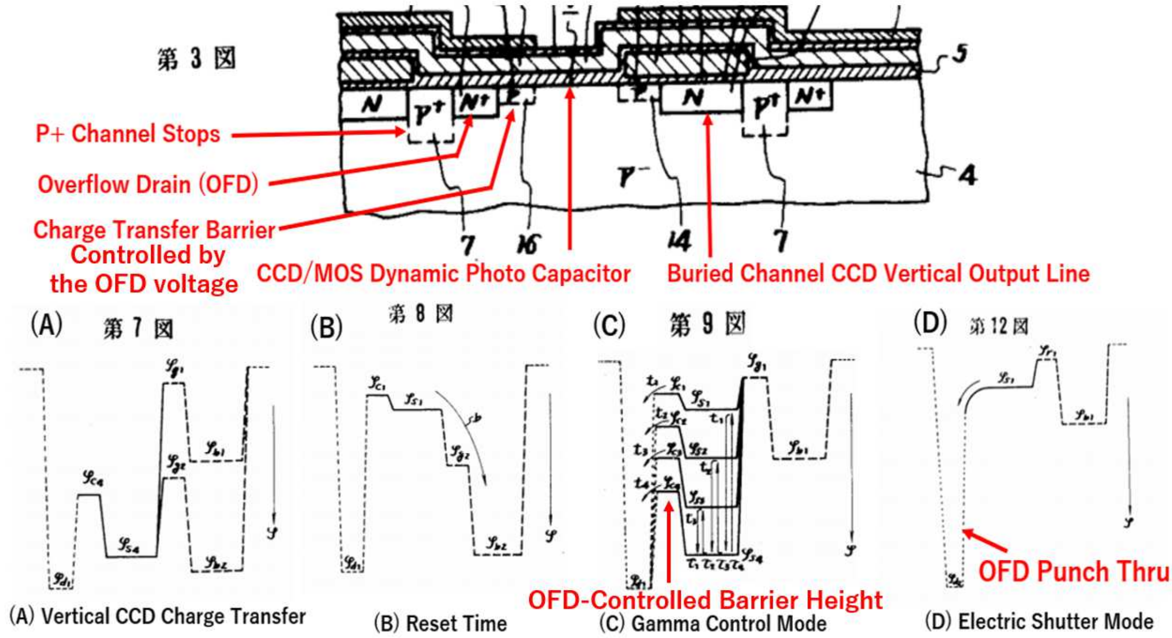


Figure 14. *Electric Shutter Function and Gamma Control defined in JPA1977-126885 patent proposed by Hagiwara in 1977.*

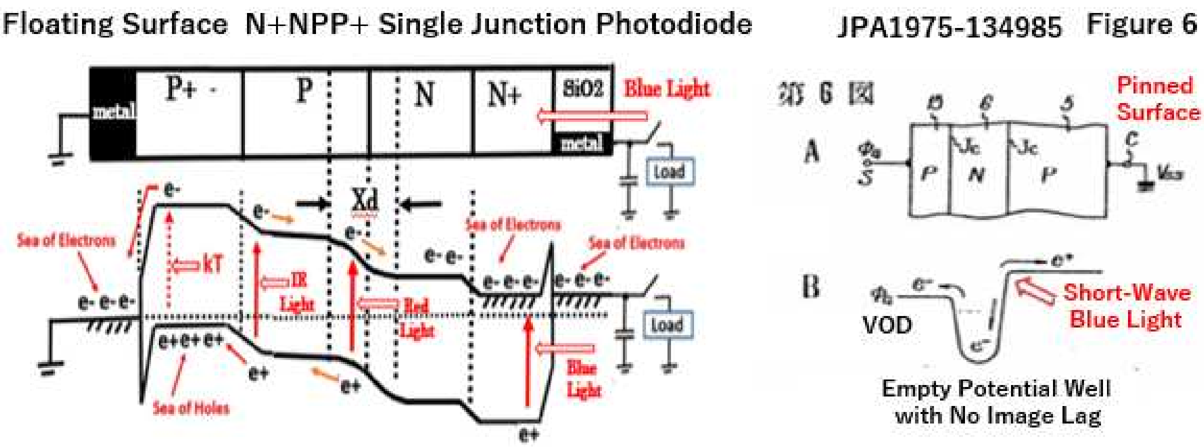


Figure 15. *Comparison of Floating Surface Single Junction Photodiode and Pinned Surface Double Junction Photodiode.*

5. Pinned P+P Surface Barrier Potential Used for Photo Electron and Hole Pair Separation

The CCD/MOS dynamic photo capacitor type photo sensor has the excellent feature of no image lag but with the serious surface dark current problem. On the other hand, the floating N+P junction photodiode has low surface dark current but with the serious image lag problem.

However, the surface pinned P+NP double junction photo transistor type and the surface pinned P+NPN triple junction photo thyristor type Pinned Photodiode invented by Hagiwara in 1975 have both of the excellent features of no serious image lag problem and no serious surface dark current problem. See

Figure 15 which shows the Pinned PNP photodiode with the empty potential well with no image lag feature as first reported in the Hagiwara SSDM1978 paper in Tokyo, Japan in 1978 [6-7]. However, the most important feature of Pinned Photodiode is the short-wave blue light sensitivity See Figure 16 which shows PNP Pinned Photodiode with an adjacent P+ channel stops formed by high-energy ion implantation.

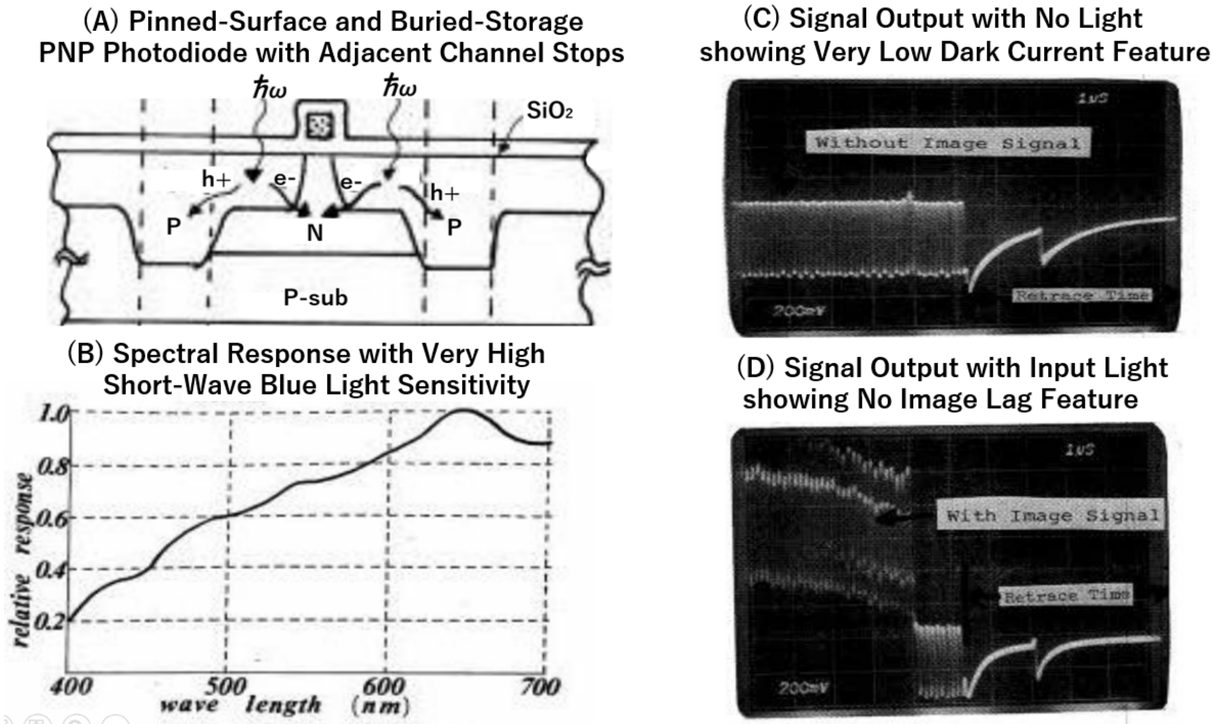


Figure 16. *The Spectral Response and Signal Outputs reported in Hagiwara SSDM1978 Paper [6-7] showing the No Image Lag Feature.*

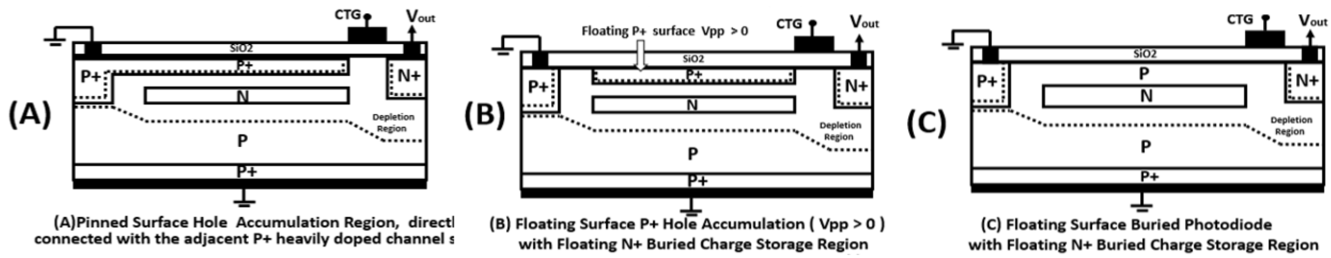


Figure 17. *Three types of PNP Double Junction type Photodiodes.*

Figure 17 shows three types of double junction type photodiodes. The slight difference of Pinned Photodiode (A) and Buried Photodiodes (B) and (C) is explained here. All of (A), (B) and (C) type photodiodes are Buried Photodiodes.

However, (B) and (C) type Buried Photodiodes are not Pinned Photodiode because the semiconductor surface is floating and being isolated and disconnected electrically from the adjacent P+ grounded channel stops.

They have the floating silicon surface being surrounded by the depletion region, which is extended from the deeply biased N charge storage region with a parasitic capacitor-coupling thru the gate oxide under the charge transfer gate (CTG) which has a very high positive value at reset time.

Consequently, the silicon surface of the type (B) and type (C) photodiodes being floating with a positive voltage, the N charge storage region itself then also becomes floating, which results in the serious image lag problems in both (B) and (C) type Buried Photodiodes.

Any photodiode, including (B) and (C), with the serious image lag problem cannot be Pinned Photodiode by definition. Any hole accumulation diode (HAD) without Pinned Surface also has the serious image lag problem and cannot be by definition Pinned Photodiode.

Pinned Photodiode must have the Pinned Surface. However, any Buried Photodiode (BPD) and Hole Accumulation Diode (HAD) with the Pinned Surface is indeed Pinned Photodiodes.

Pinned Photodiode can be formed either by pinning the P+ surface hole accumulation region either by the adjacent heavily dope P+ channel stops as developed and reported in the SSDM1978 paper by Hagiwara in 1978 or by the direct metal contact as an option as proposed in the 1975 Japanese Patent Application JPA1975-134985 by Hagiwara.

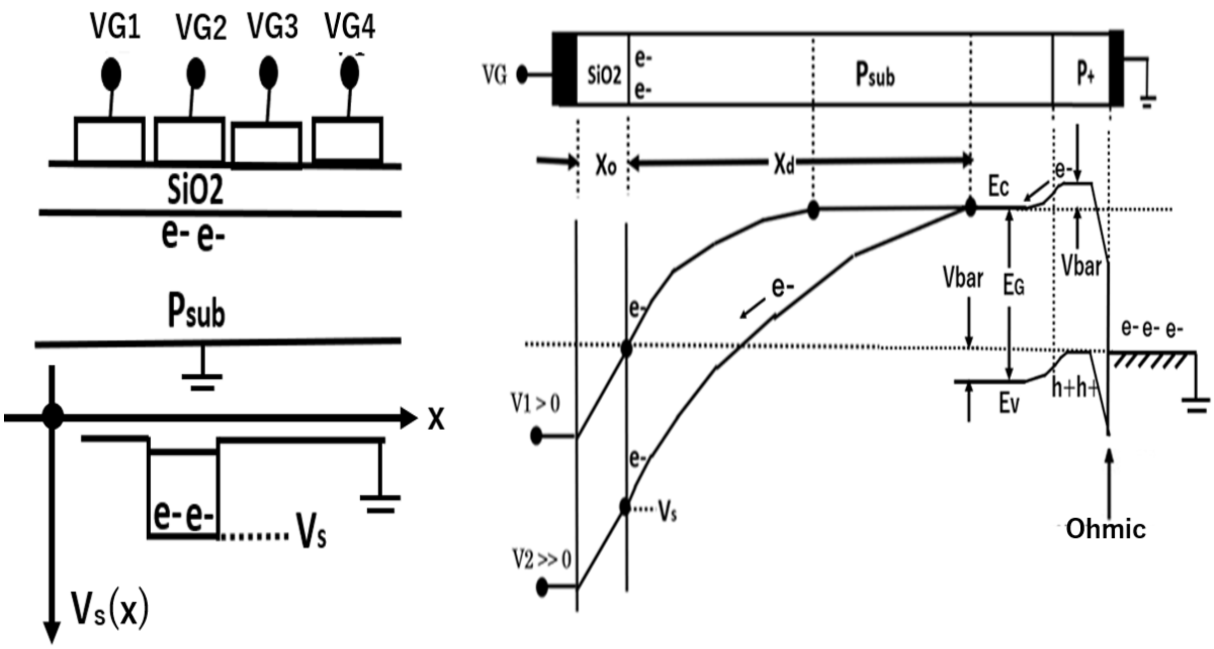


Figure 18. Electron Potential Profile of Surface Channel CCD.

Figure 18 shows a simple CCD/MOS dynamic photo capacitor used for surface channel CCD. At a small positive gate voltage, the semiconductor surface can be inverted to form an inversion layer for mobile electrons to move along the surface inversion channel. In this case, the thicker the gate oxide, the weaker the influence of the gate voltage over the surface inversion channel potential, resulting in a shallower surface potential.

Figure 19 shows the BCCD/MOS dynamic photo capacitor used for buried channel CCD. In this case, on the other hand, when the gate oxide is made thicker, the minimum buried channel potential V_m becomes deeper, and when the gate voltage VG is set at a strong negative value. the surface potential Vs will be pinned at the grounded substrate voltage creating the surface hole accumulation region. The concept of Pinned Surface Potential and the hole accumulation diode (HAD) has an origin in the buried channel CCD structure.

In both Figures 18 and 19, the heavily doped P+ region is formed at the back of the wafer to make the ohmic ground contact. As a result, the barrier potential $V_{bar} = kT \ln (N_{aa}/N_a)$ is created by the P+P doping profile, where N_{aa} is the doping level of the heavily doped P+ region and N_a is the doping level of the P type substrate. Naturally the P type substrate potential must be pinned to the ground reference voltage connected by a metal ground contact. It was a very natural choice to form a Pinned Photodiode for back-light illumination image sensors.

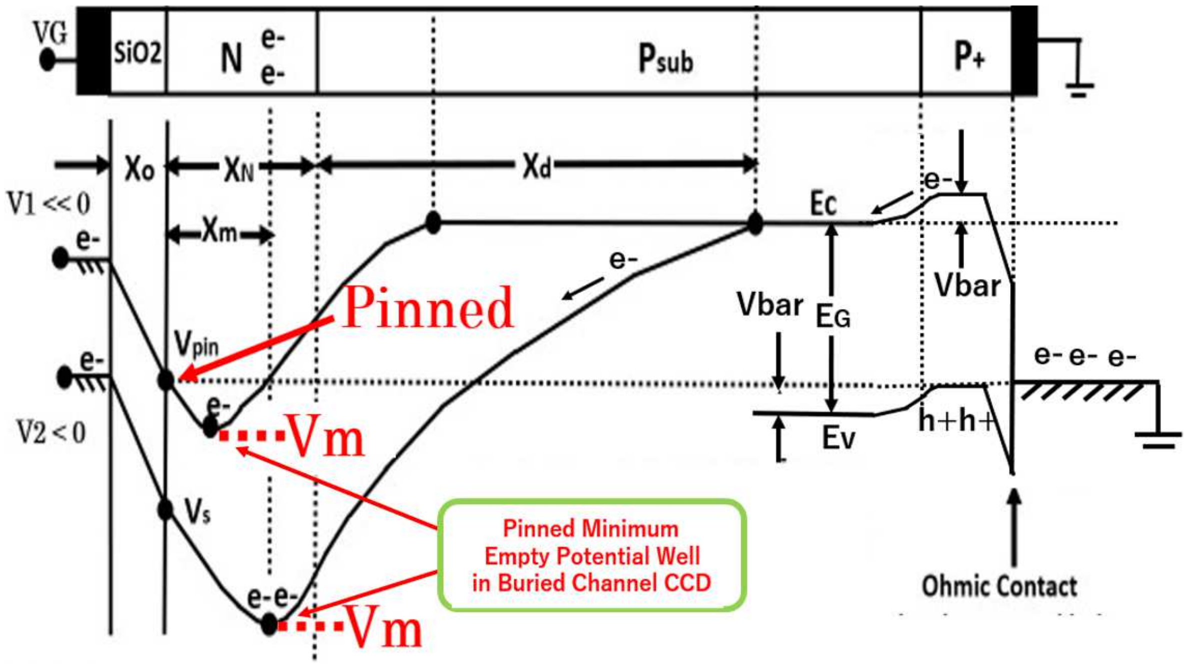


Figure 19. Electron Potential Profile of Buried Channel CCD.

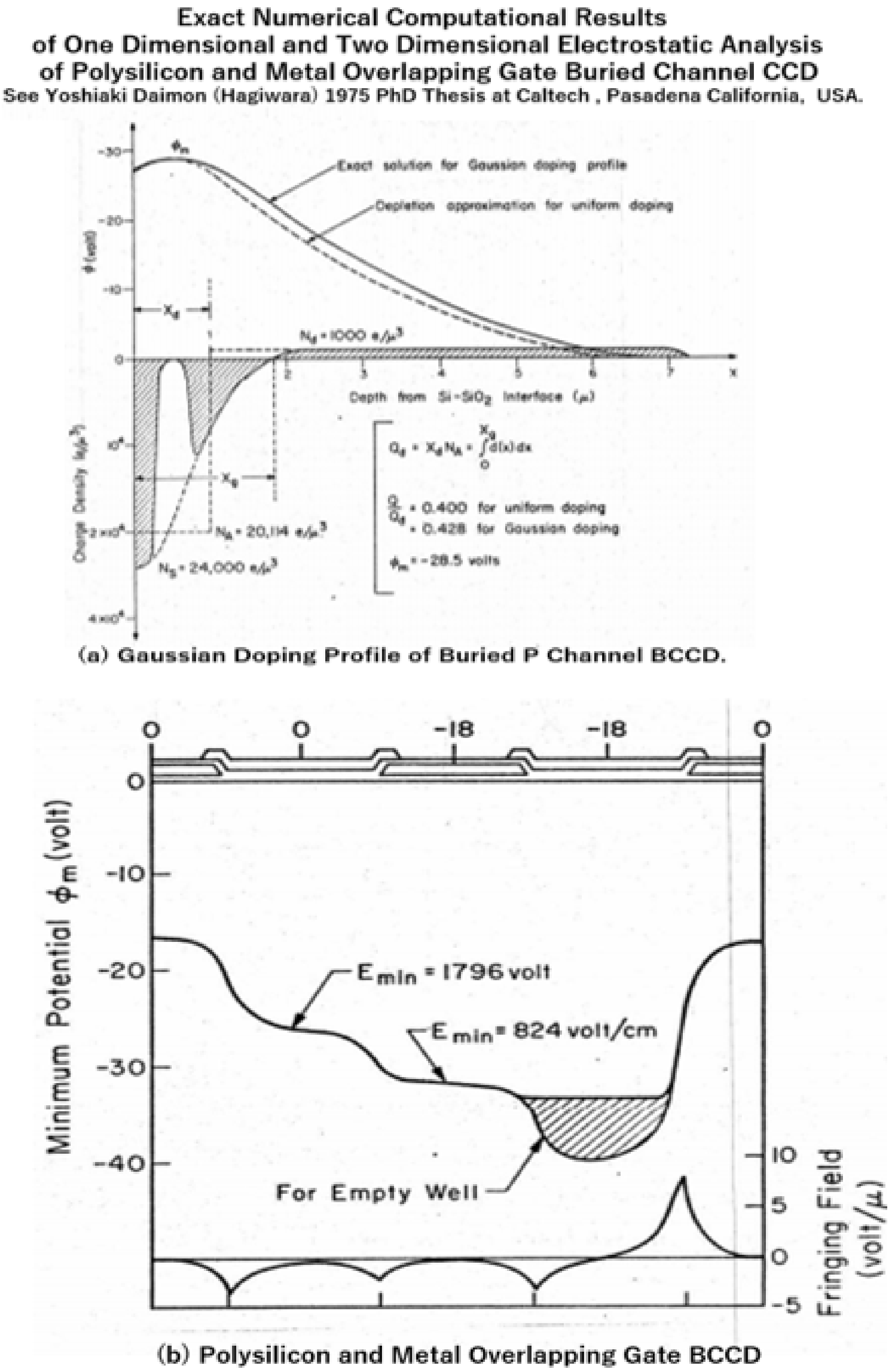


Figure 20. Electron Potential Profiles of Buried Channel CCD.

6. Numerical Computation of Electrostatic Potentials of Buried Channel CCD and Pinned Buried Photodiode

Figure 20 shows the results of numerical computations of the Gaussian doping profile and the signal charge distribution with the two-dimensional electrostatic static potential profile of the overlapping gate buried channel CCD structure [15].

Figure 21 shows how the signal charge flows in a Buried Channel Charge Coupled Device (BCCD) which has much faster charge transfer capability with the excellent charge transfer efficiency of about 99.999%. A computer graphics of film motion picture was generated by an exact numerical computation at JPL/Caltech, Pasadena, California, USA. And the movie was reported in the IEEE ISSCC1974 technical conference on February 1974 in Philadelphia, USA. It was a part of PhD thesis by the author.

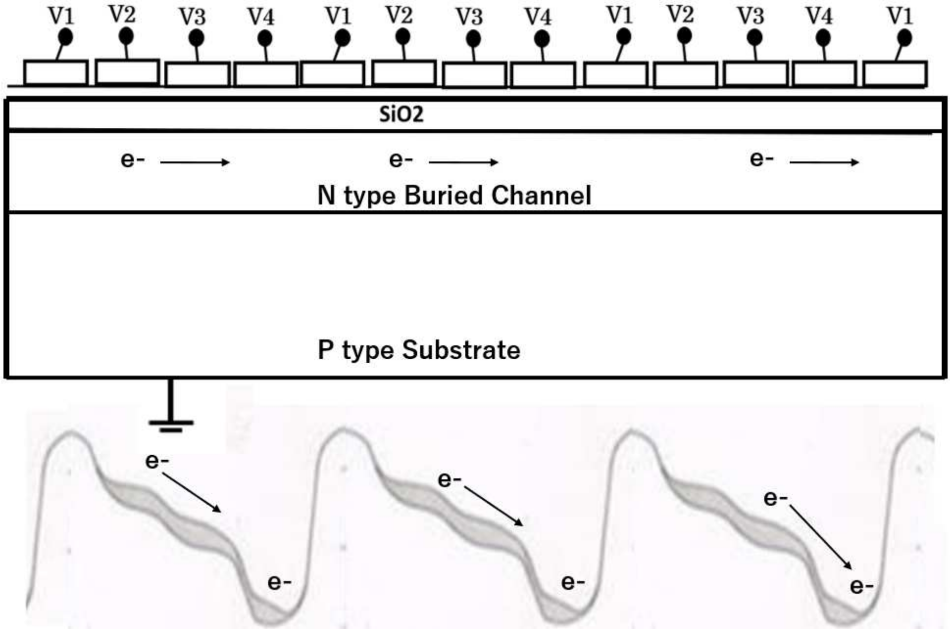


Figure 21. *Buried Channel type CCD structure and its potential profile.*

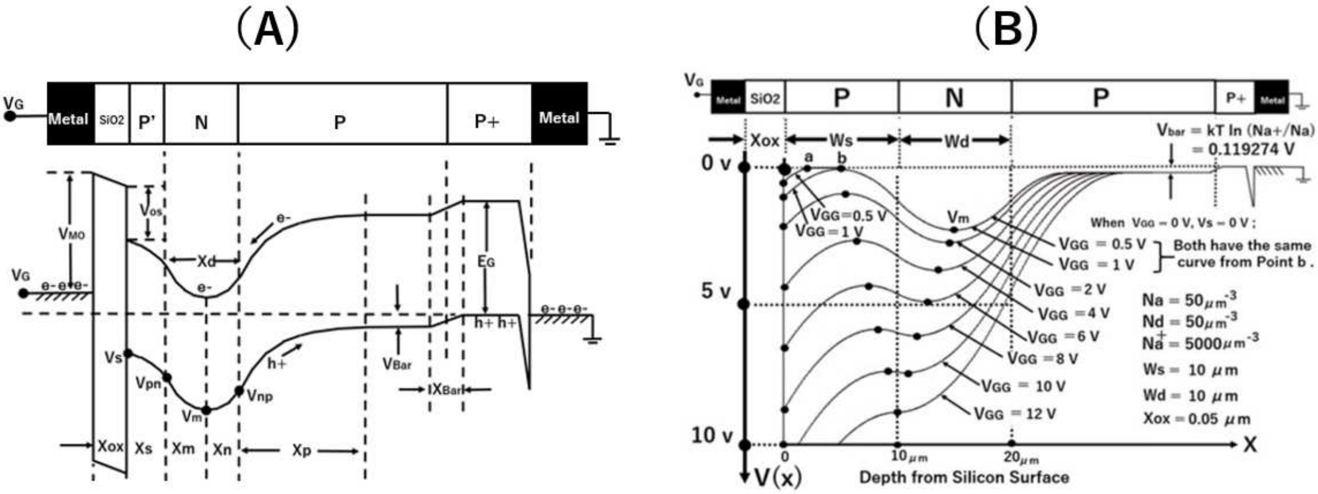


Figure 22. *Double Junction P+PNP type Pinned Photodiode with CCD/MOS Dynamic Buffer Memory Capacitor.*

Figure 22 shows the electrostatic potential profiles V(x) of the double junction P+PNP type Pinned and Buried Photodiode with back-light illumination mode, which was originally invented in 1975 by Hagiwara. The photo electron charge is generated at the back semiconductor surface, stored in the buried N-type charge storage region and then transferred to the CCD/MOS dynamic buffer memory capacitance at the front semiconductor surface. The gate voltage V_{GG} of the CCD/MOS dynamic buffer memory capacitance for the Global Shutter operation mode was used as a parameter for the potential profiles.

For a small value of the gate voltage, there is an empty potential with the minimum potential value of V_m in the buried N type charge storage region. The photo electrons generated at the silicon surface at the back are led to the empty potential well and stored. When the gate voltage V_{GG} becomes a positively large voltage, by the punch-thru operation mode, the photo electron charge stored in the N-type buried storage region will be all drained to the inverted surface of the CCD/MOS dynamic buffer memory capacitance at the front side.

Without an extra in-pixel buffer memory, the conventional CMOS image sensors suffer the rotary shutter effect and the pictures with moving objects are distorted. See Figure 23.

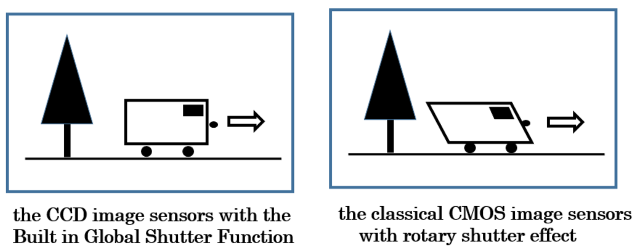


Figure 23. *Undesired Rotary Shutter Effect of Conventional CMOS Image Sensors.*

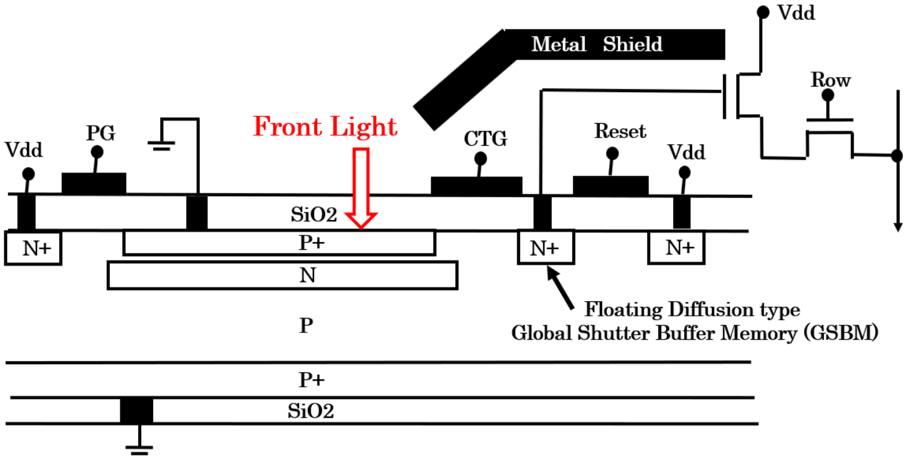


Figure 24. Floating Diffusion Type Global Shutter Buffer Memory used for In-Pixel Active Sensor.

As another option, instead of the CCD/MOS dynamic photo capacitor type Global Shutter buffer memory, Figure 24 shows a floating diffusion (FD) type Global Shutter buffer memory which is equipped with an in-pixel active photo sensor with the source follower current amplifier read-out circuit and with the double junction P+PNPP+ type Pinned Photodiode P+ pinned surface and the buried N type photo electron charge storage region.

Figure 25 shows a schematic of the snap-shot active photodiode with the floating diffusion (FD) type Global Shutter buffer memory, which was developed and reported by Pain Team in Caltech/JPL in 1998. In this example the photo sensor structure was not the type of Pinned Photodiode with the Pinned P+ surface proposed by Hagiwara in 1975 but this structure can be fabricated with the conventional CMOS process which is widely used for digital LSI chips and cost-wise very attractive [16].

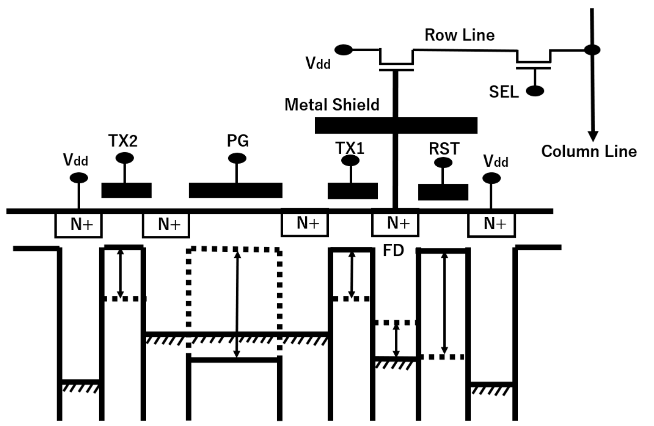


Figure 25. Undesired Rotary Shutter Effect of Conventional CMOS Image Sensors.

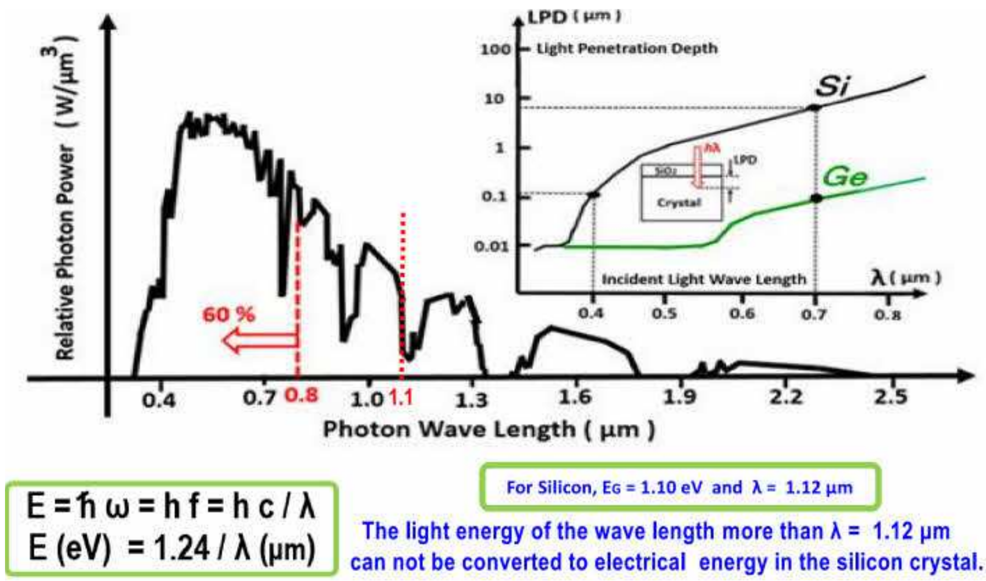


Figure 26. Photo Energy Spectrum of Sun Light and Light Penetration Depth of Silicon Crystal.

It is not well understood that the depletion region of the PN junction is not the only place where we can achieve photo electron and hole pair separations effectively. As shown in Figure 26, the short-wave blue light has only 1000Å silicon crystal penetration depth. The pinned surface P+P Gaussian doping profile has a very important role to achieve a better photon to energy conversion efficiency, especially for the short-wave blue light. In this paper now, the electrostatic and dynamic behaviors of Pinned Surface P+PNP Double Junction type Dynamic Photo Transistor and Pinned Surface P+PNPN Triple Junction type Dynamic Photo Thyristor are analyzed in details. Both of them are shown to be expected to have much excellent photon to electron energy conversion efficiency. It is concluded that the actual real Pinned Photodiode refined in production are also of the P+PNP junction type photodiode which can also be used for new type of solar cells with a much higher photon to electron energy conversion efficiency. Figure 27 shows the results of the numerical calculations of the P+P Barrier Potential V_{bar} and the actual barrier width W_{BAR}. In analogy of the P+P barrier potential of the drift field transistor as shown in Figure 12, and by Debye Length approximation, we had the total barrier width as $W_{bar} = L_{dd} + L_d = 637$ Å, where L_{dd} is Debye Length for the doping level of N_{aa} while L_d is for N_a. Actual barrier width W_{BAR} was found to be about three times wider than the rough estimation W_{bar}. That is, we have $W_{BAR} = 3\ W_{bar} = 3\ (L_{dd} + L_d) = 1912$Å which is very wide.

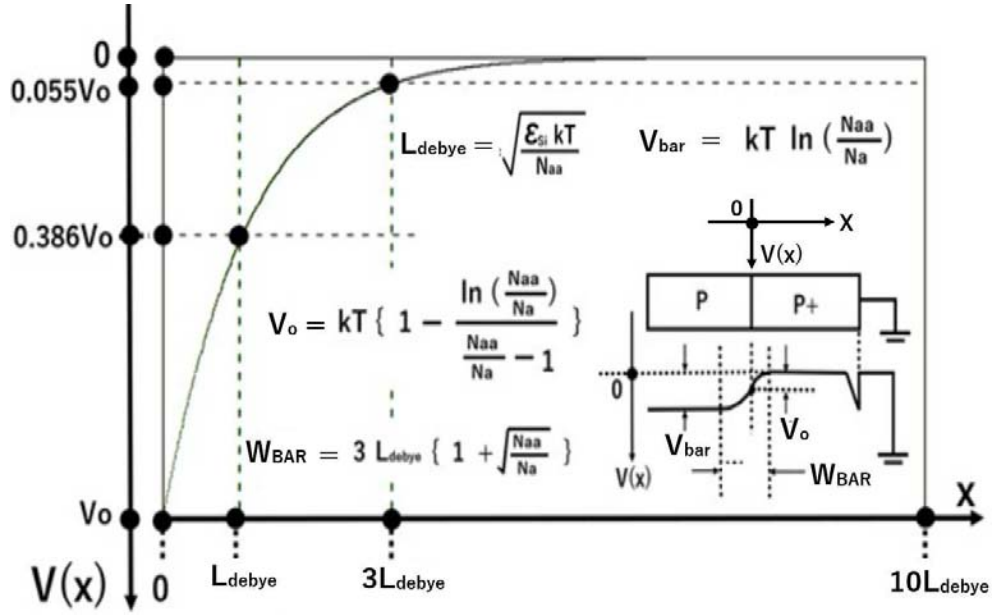


Figure 27. *Barrier Potential and Barrier Width of P+P Doping Profile.*

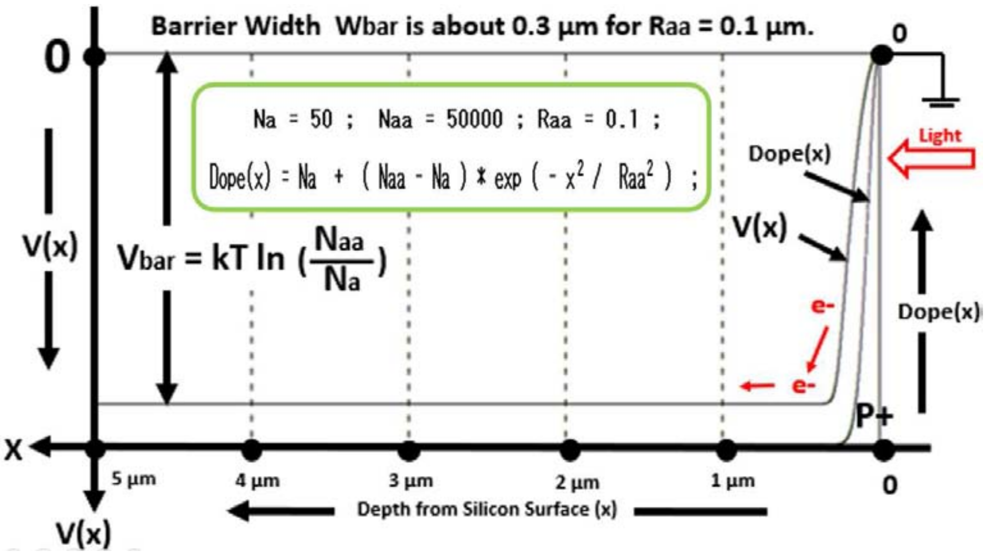


Figure 28. *Barrier Potential and Barrier Width of P+P Single Gaussian Doping Profile.*

Figure 28 shows the exact numerical value of the barrier potential V(x) as a function of the distance x from the semiconductor surface for a single Gaussian doping profile $Dope1(x) = (N_{aa} - N_a)\ exp\ (-\ x^2 / R_{aa}{}^2) + N_a$ with the surface doping density of $N_{aa} = 5000\ \mu m^{-3}$ and the spread parameter $R_{aa} = 0.1\ \mu m$.

The normalized doping profile Dope(x) is plotted with the normalization by the value $Dope1(0) = N_{aa}$ at the semiconductor surface (x = 0). As expected, the barrier potential width W_{BAR} was found to be about three times wider than the spread parameter of $R_{aa} = 0.1$ µm.

Figure 29 shows the exact numerical-computation results of the barrier potential V(x) for a double Gaussian doping profile $Dope2(x) = N_{aaa} \exp(-x^2/R_{aaa}^2) + Dope1(x)$ with $N_{aaa} = 3000$ µm $^{-3}$. The normalized doping profile Dope(x) is plotted with the value $Dope2(0) = N_{aa}$ at the semiconductor surface (x = 0).

As expected, the barrier potential width W_{BAR} was found to be about $W_{BAR} = 3W_{bar} = 3$ µm, which is about three times wider than the spread parameter of $R_{aaa} = 1$ µm for Figure 28.

The barrier potential profile V(x) was found to be very close to the approximated value of V1(x) = kT ln (Naa / Dope1(x)) for the case of the single Gaussian doping profile in Figure 27 and V2(x) = kT ln (Naa / Dope2(x)) for the case of the double Gaussian doping profile in Figure 28.

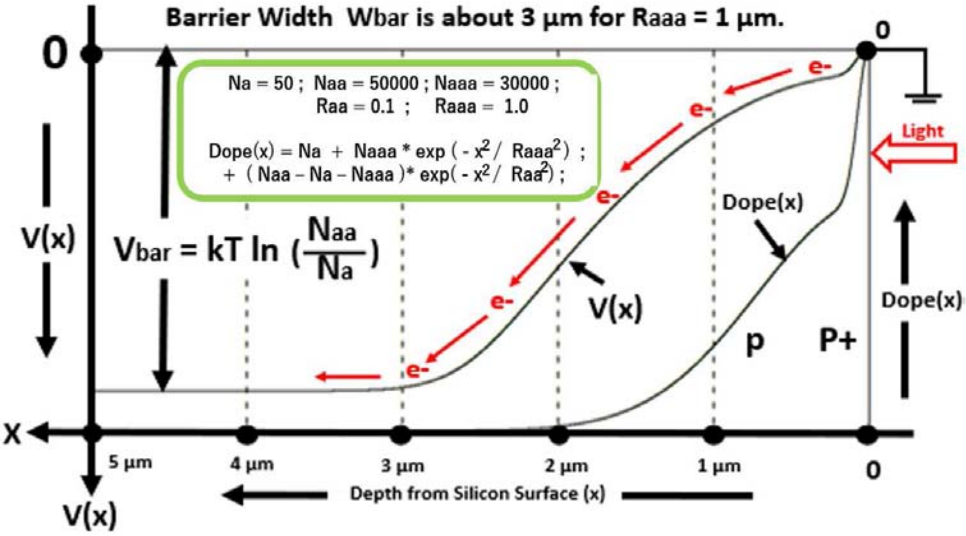


Figure 29. *Barrier Potential and Barrier Width of P+P Double Gaussian Doping Profile*

7. Pinned and Buried Photodiode Type Double Junction P+PNPP+ Solar Cell

Figure 30 shows four types of image sensor structures. They are (a) the conventional N+NPP+ single junction photo sensor with the N+ floating surface with the problem of incomplete charge transfer and serious image lag problems, (b) the conventional P+PNN+ single junction photo sensor with the N+ floating surface with the problem of incomplete charge transfer and serious image lag problems, (c) the single junction N+NPP+ type Solar Cell with the pinned N+ surface type Pinned Photodiode, and (d) the new solar cell structure proposed by Hagiwara in 2020 using the P+PNPP+ double junction type Pinned Photodiode.

It is not well known that both (c) and (d) type photodiode structures were originally invented by Hagiwara at Sony in 1975 in Japanese Patent Application JPA1975-127646, JPA1975-127647 and JPA1975-134985. Unfortunately, these patent applications were written in Japanese and, having never been applied in oversea patents, were never exposed to the English-speaking community. Consequently, it is not well known world-wide that Pinned Photodiode was originally invented by Hagiwara at Sony in 1975. Most of high-performance image sensors now use Pinned Photodiode structure invented by Hagiwara in 1975. This is not a story of the past. The concept of the P+ Pinned surface for the photosensor also has a potential future application as Pinned Photodiode Type Solar Cell with better photo-to-electron energy conversion efficiency [17].

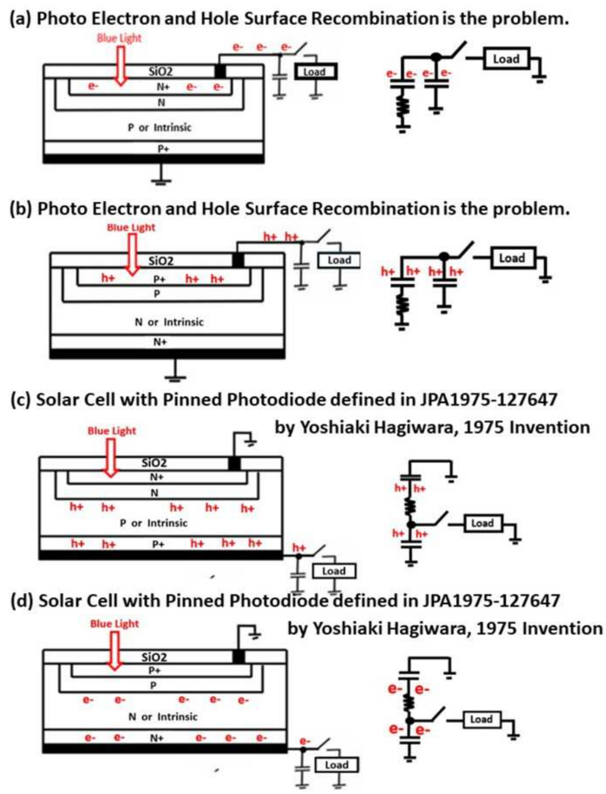


Figure 30. *Comparison of Single and Double Junction Type Image Sensors and Solar Cells.*

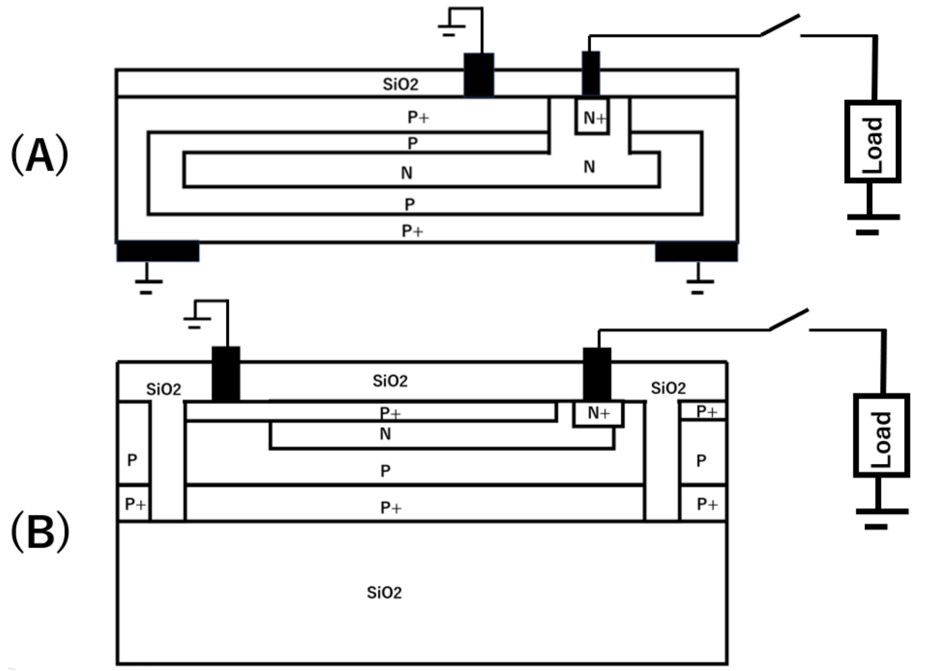


Figure 31. *The P+PNP+ Double junction type Solar Cell Structures with the P+ Pinned Surface of Hole Accumulation Thin Layer of Less Than 500 Å.*

Figure 31 shows two kinds of the P+PNP+ double junction type solar cell structures with the pinned P+ surface of Hole Accumulation region of less than 500 Å. The total P+ dosage must be more than 3 x 10^{13} cm^{-2}.

Figure 32 shows a schematic of four Pinned Photodiode type solar cells in series connection. The total solar cell output voltage V_{OUT} in this case is about V_{OUT} = 2 E_G. Since the output voltage of a single solar cell is always less than E_G and is approximated here as $E_G/2$.

In case of the type (A) solar cell structures, the P type substrate of each solar cell device unit cannot be electrically isolated from each other by a common N region for isolation because as the photo electron charges are accumulated in the buried N type photo charge storage region, each N region will become negatively biased. Each solar cell unit must be cut and assembled as a single chip. Consequently, four solar cell unit chips are needed to obtain the output voltage of V_{OUT} = 2 E_G.

For cost-wise, the polysilicon solar cells of type (B) on the cheap insulator base (SiO_2) films are very attractive. Besides, the SiO_2 insulator can isolate the substrate of each solar cell device unit electrically, and many solar cell units can be fabricated on the same single SOI wafer at the same time.

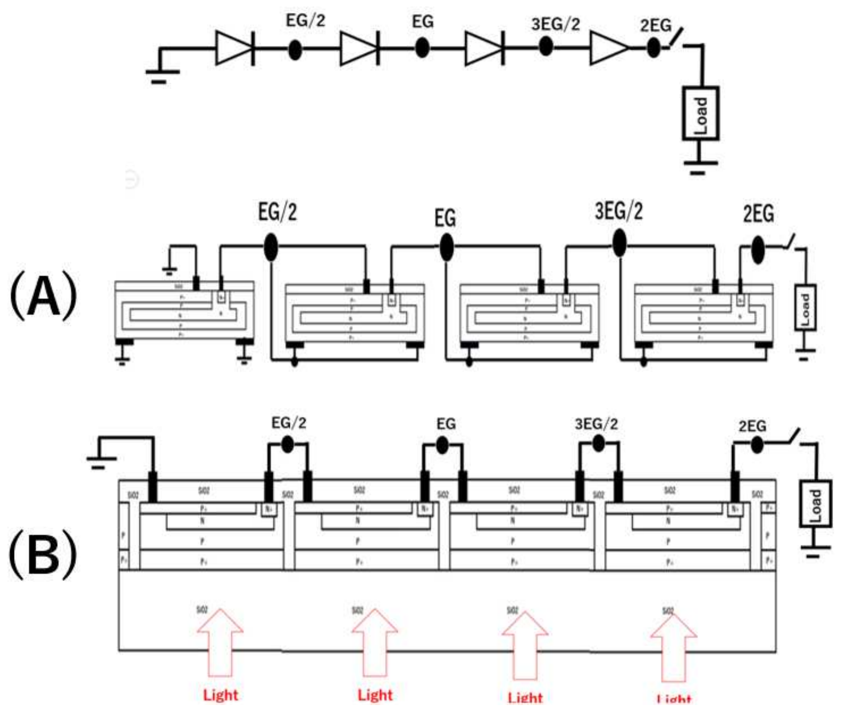


Figure 32. *Four Pinned Photodiode Type Solar Cells in Series Connection.*

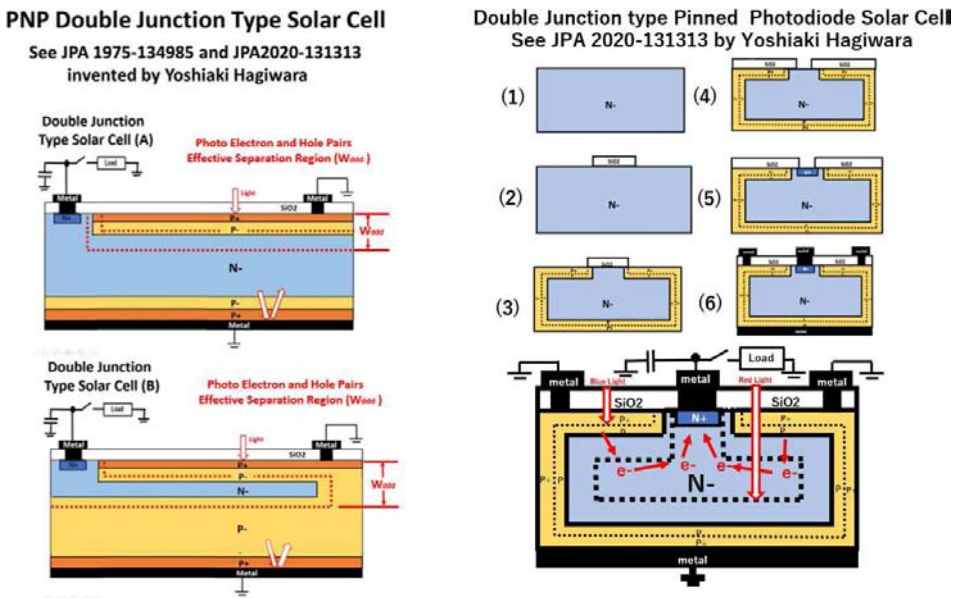


Figure 33. Fabrication Process Flow of Double Junction P+PNPP+ Solar Cell.

Figure 33 shows an example of the fabrication process flows of the double junction P+PNPP+ type solar cell. Figure 34 compares the conventional N+P single junction type solar cell (A) and (B) with the floating N+ surface and the new solar cell of the P+PNPP+ double junction type solar cell (C) and (D) proposed by Hagiwara 2020. The buried N-type region collecting the photo electrons are always empty with the empty potential well since the photo electrons are all drained to the N+ diffusion charge storage capacitance, which has the maximum output voltage of V_{out} = 0.2 volt in this device design which is very small. But by a proper design of the optimum doping profile of the N type buried region, theoretically the maximum output voltage V_{out} near E_G = 1.1 eV is possible.

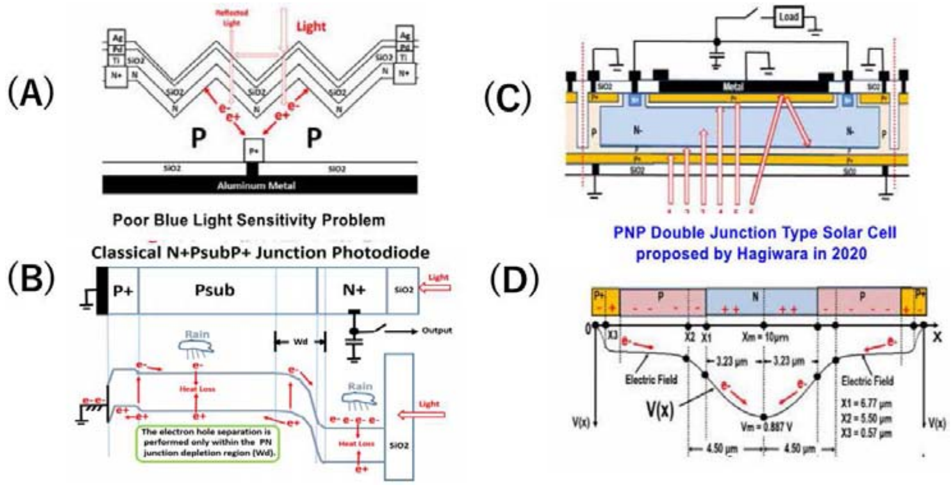


Figure 34. Fabrication Process Flow of Double Junction P+PNPP+ Solar Cell.

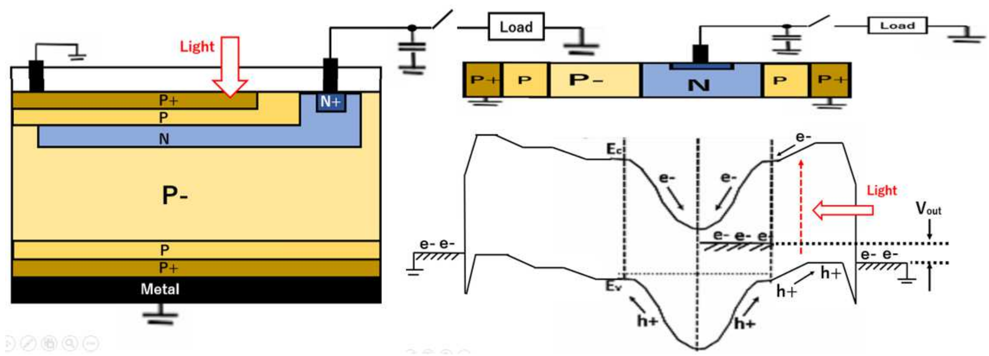


Figure 35. Band Diagram of P+PNPP+ Double Junction Type Photodiode Solar Cell.

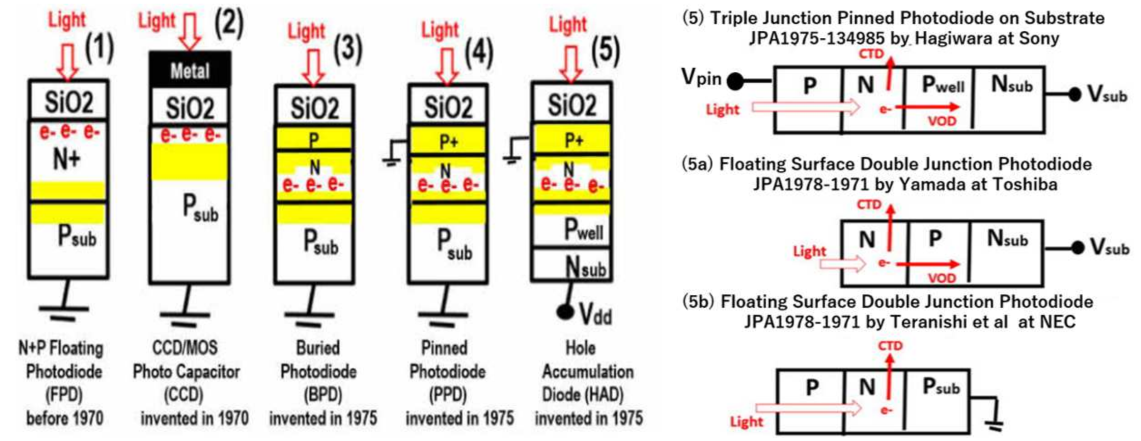


Figure 36. *Historical Developments of Five types of Basic Photo Sensors Structures.*

Figure 35 shows a band diagram of a P+PNPP+ Double Junction type Pinned Photodiode Solar Cell structure and the corresponding band diagram of the empty potential well profile. The sum of the depth of the minimum potential V_m and the solar cell output voltage V_{out} must be less than the silicon band gap energy E_G. That is, we have $V_m + V_{out} < E_G$.

Figure 36 shows historical developments of five types of basic photosensors. The floating N+ surface single N+P junction photodiode (1) was prevailing before the invention of the CCD type PPD and CTD (2). In 1975 Hagiwara invented (3), (4) and (5) types of the Pinned Photodiode with the pinned P+ surface of hole accumulation. Hagiwara team at Sony developed in 1978 the type (4) Pinned Photodiode and used it in a FT CCD image sensor and reported the results in SSDDM1978 conference in Tokyo, Japan in 1978.

In 1982, Teranishi team at NEC developed the buried photodiode of type (3), used in a ILT CCD image sensor. and reported the serious image lag problem in IEDM1982 conference. KODAK team developed the type (4) photo sensor, used it in an ILT CCD image sensor and reported IEDM1982 conference. KODAK named as Pinned Photodiode.

The complete form of the type (5) photodiode with the PNPN thyristor punch-thru action mode with the snap-shut electrical shutter function was developed by Hamazaki team at Sony in 1987. Sony named the type (5) photo sensor as Hole Accumulation Diode (HAD). But NEC Buried Photodiode (BPD) of type (3), KODAK Pinned Photodiode (PPD) of type (4) and Sony Hole Accumulation Diode (HAD) of type (5) are all identical to the photodiodes defined in the three Japanese patent applications, JPA1975-127646, JPA1975-127647 and JPA1975-134985 proposed by Hagiwara at Sony originally.

Figure 37 shows a comparison of Sony 1978, NEC 1982 and Kodak 1984 Photodiodes. By necessity, Pinned Photodiode needs an adjacent heavily doped P+ channel stops to supply hole carriers into the surface P+ region. Otherwise, the surface P+ region cannot be pinned and fixed at the substrate ground voltage level.

Apparently, KODAK IEDM1984 photodiode has the adjacent LOCOS region directly connected to the P+ hole accumulation region of the photo sensor. And this is actually the definition of Pinned Photodiode. However, apparently NEC IEDM1982 photodiode does not have the adjacent P+ heavily doped channel stops, and the surface P+ region may be surrounded and isolated electrically by the depletion region extended by the buried N charge storage region.

Any floating source region cannot be drained completely of signal photo electron charge and suffers the serious image lag problem. That is why the NEC IEDM1982 paper reported the serious image lag problem. See also Figure 7 for confirmation.

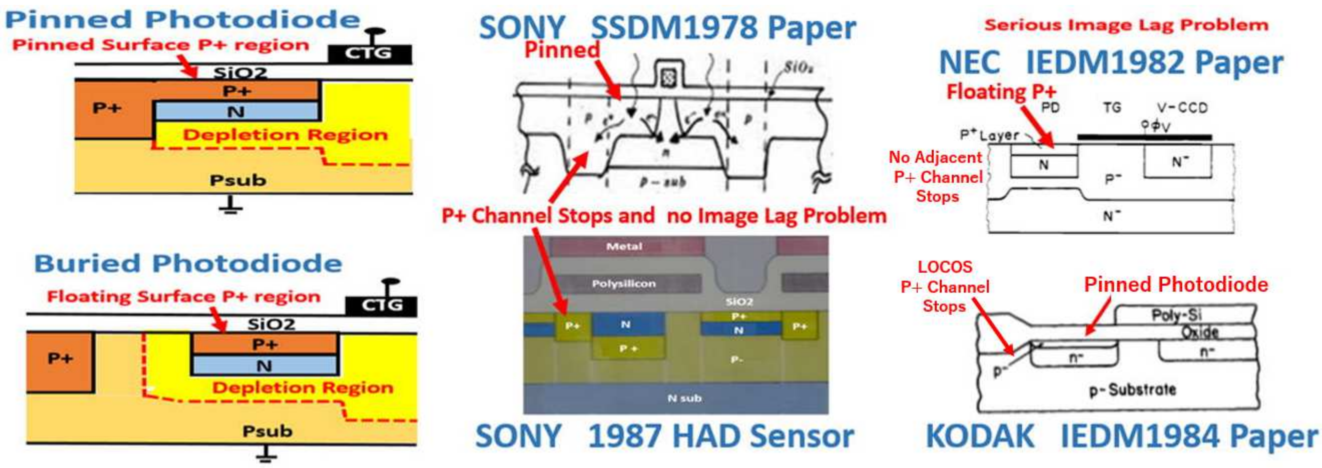


Figure 37. *Comparison of Sony 1978, NEC 1982 and Kodak 1984 Photodiodes.*

The silicon crystal penetration depth of the high photon energy short-wave blue light is about 0.1µm. Besides, the edge of the depletion region of a floating surface N+P junction type photodiode is located at least a few µm in depth beneath the silicon crystal surface. Hence the short-wave blue light with high photon energy cannot reach the depletion region of the PN junction. Only the relatively-long wave-length light with a low photon energy can be converted into the electron energy in the PN junction depletion region of the very narrow width Xd. This is the main reason why the conventional floating surface N+P junction type Solar cell has a relatively low photo-to-electron energy conversion efficiency. With the same reason, the classical simple N+P single floating junction photodiode used in the MOS type CTD image sensors had a poor short blue light sensitivity. So is the conventional N+P junction type solar cell of low efficiency. The sun light is very rich with the short-wave high energy photons. If the heavily doped P+P profile with the barrier potential of kT ln (N_{aa} /N_a) is formed at the silicon surface of the light illumination side, the short-wave blue light also contributes the solar cell photon energy conversion efficiency. The double junction P+NP type dynamic photo transistor has been intensively studied and well understood now, being powered by the image sensor market. The most important feature of the double junction P+NP type dynamic photo transistor is the complete charge transfer without a single photo electron loss. However, if the double junction type dynamic photo transistor is used for the future solar cells in a proper process and device design, a single photo electron over 1.1 eV energy may not be lost with a very high photon-to-electron energy conversion efficiency.

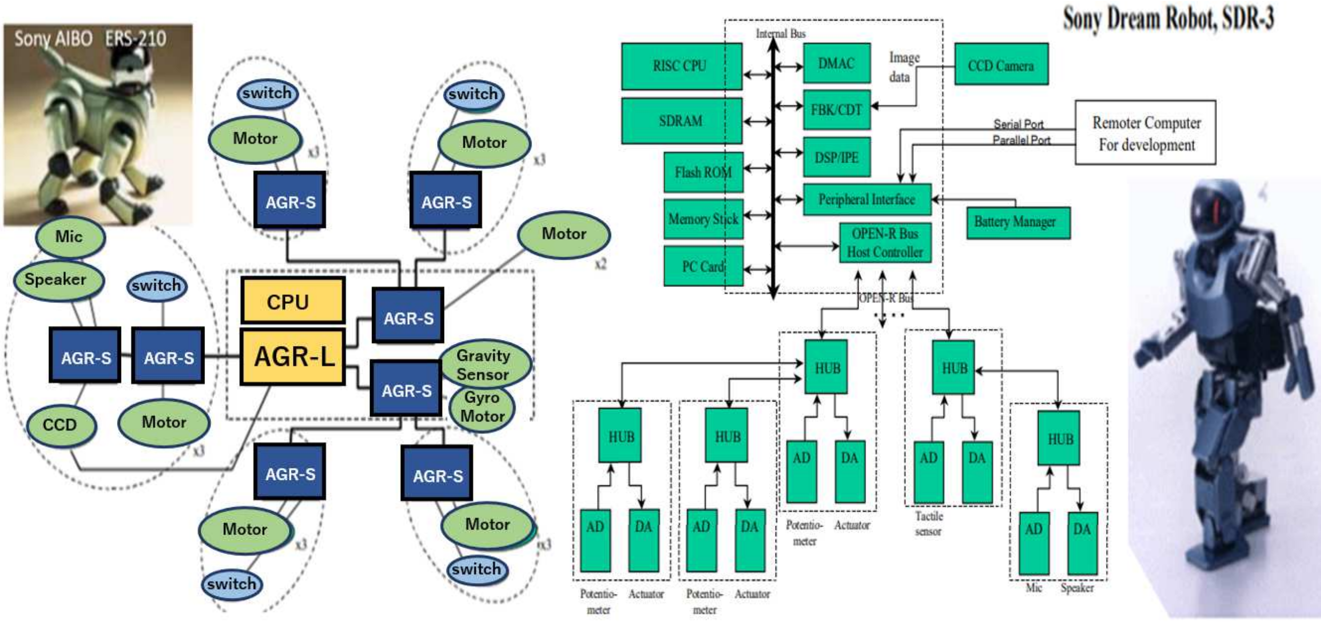


Figure 38. *Sony Dream Robot AIBO ERS-210 and SDR-3.*

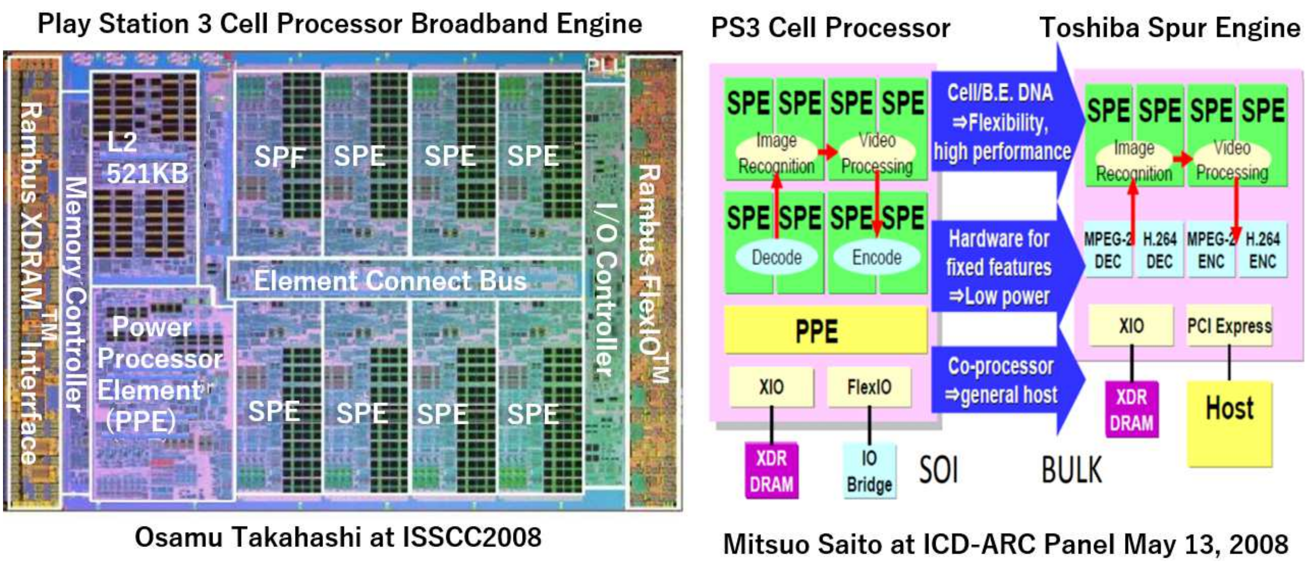


Figure 39. *PS3 Cell / B. E. and Toshiba Spurs Engine.*

8. Future of Intelligent Image Sensor System

Figure 38 showed the AIBO robot system which was made possible with many important semiconductor LSI chip components including the intelligent image sensor chips and the rotary encoder DSP chips for controlling the movements of robot arms. Semiconductor LSI chips are essential supporting components for the human civilization.

In 2001 Hagiwara was invited in the International Conference ESSCIRC2001 in Vilach, Austria to talk about his life works and his dream on the entertainment consumer products [18].

In 2008 Hagiwara was again invited in the International Conference ESSCIRC2008 in Edinburgh, Scotland U. K. to talk about his dream on the entertainment consumer products including the real time fast dedicated cell processor engines, which include the Cell / B. E. and Toshiba Spurs for the PS3 game machine [19]. See Figure 39.

Like a human brain with the feedback system of the left and right brains helping and communicating with each other for the same goal and destiny in single unit body, the artificial intelligent image sensors need the pair of the left and right identical AI processing units with high performance CMOS digital circuits and clever software engines. The visitor counter system with the two vision cameras to judge and detect the flow direction of the moving visitors is also a real time hardware engine with the clever design of the analog and digital circuits helping the task of the artificial intelligent image sensor.

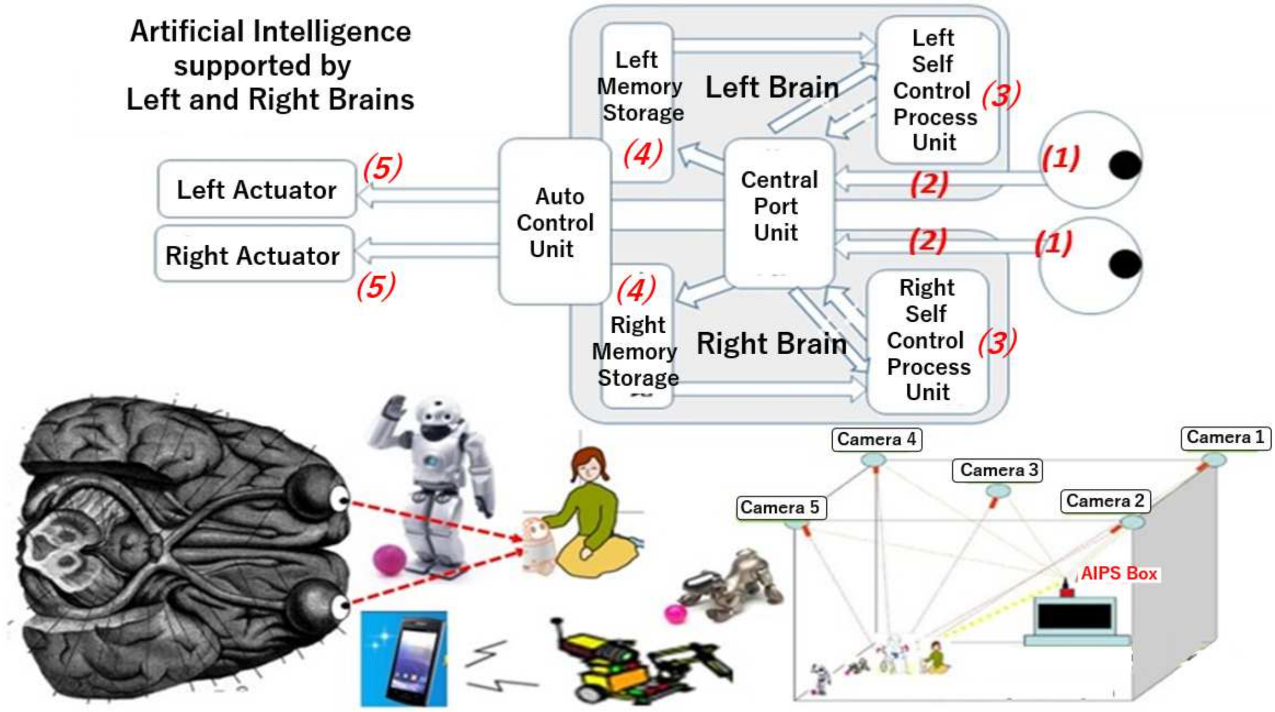


Figure 40. *Artificial Intelligence supported by Left and Right Brains.*

Many Artificial Intelligent Image Sensors are needed to be built for home care and assistant system, together with many dedicated real time hardware engines. The servomotor controlled digital feedback system is essential not only to build a robot vision real time system but also to a self-driving car real time system. The future of the intelligent image sensor also depends strongly on the future advancement of the 3-D multi-chip interconnection technology [20-21].

Even for directing an image sensor being pin-pointed to the right object quickly in real time, many tools including high performance CMOS digital circuits and clever software designs are needed. Figure 40 shows an Artificial Intelligence Partner System (AIPS) composed of Left and Right Brain Digital Circuit systems which cannot be realized without the advanced technology of the 3-D Multi-chip LSI interconnection and semiconductor wafer process [22-23].

For related innovative inventions and improvements of circuit noise reduction techniques for the better performance of modern CMOS image sensors, see also [24-28].

9. Conclusion

Historical development and research efforts of image sensors were reviewed in details. Image sensors and solar cells are both the photon detecting device (PPD) and operate with the same physical principle of photon energy to electron energy conversion. Improvements of Image sensors for the quest of high quality and performance was discussed.

It is concluded that a typical classical image sensor was simply composed of a single N+P floating junction type photon detecting device (PDD) and has the serious image lag problem and moreover the short-wave blue light sensitivity is not satisfactory. Solar cells stay even now in the most primitive and simple form of a single N+P floating junction type photon detecting device (PDD) for the reason of the solar cell market size and the low cost of fabrication process. The photo sensor structures proposed originally by Hagiwara at Sony in 1975 are identical to NEC BPD, KODAK PPD and Sony HAD. BPD may not have complete charge transfer mode and may have the serious image lag while PPD has no image lag feature. PPD also has the very low surface dark current feature and the excellent blue light sensitivity feature.

The double and triple junction type Pinned and Buried Photodiode with the P+P surface hole accumulation invented and defined in Japanese Patent Applications by Hagiwara in 1975 were the right solution to improve the performance of image sensors and solar cells. The digital CMOS video cameras, with all solid state, film free, mechanical parts free, high definition and low power features, now transformed the image sensor world from an analog life style to a digital life style completely.

Acknowledgements

The author expresses sincere gratitude to Prof. James McCaldin at California Institute of Technology (Caltech) for introducing and teaching Hagiwara the basic semiconductor device physics at Caltech in 1969 with a plenty of side-wall back-ground exciting stories of the Intel self-aligned MOS transistor technology and the newly developed high energy ion implantation technology. The author also expresses sincere gratitude to Prof. C. A. Mead and Prof. T. C. McGill at Caltech, for advising the original 1971 undergraduate work on the Ga_2O_3 – Au Schottky Barrier interface study and characterization, and for guiding the 1974 PhD thesis work on the Charge Transfer Analysis of Buried Channel CCD Image sensors. When the author was a PhD student of Prof. C. A. Mead at Caltech. Gordon Moore and Andy Grove both frequently visited Prof. C. A. Mead and influenced the researchers and PhD students in Prof. C. A. Mead ‘s Lab.

Sony Image Sensor R/D efforts started in 1969 with the strong initiative of the Ex-President of Sony Corporation, Kazuo Iwama, who emphasized the market need of the portable small video camera with no image lag feature for the fast-action and snap-shot pictures. Kazuo Iwama gave Hagiwara also a chance to work at Sony in 1975 to build an artificial intelligent image sensor system with the real time robot vision and the powerful digital circuit engines for real time operations. Under the guidance of Dr. Sei-ichi Watanabe, Hagiwara and his team of Miyaji and Nakagawara developed in 1989 for the first time in the world the 25-nano sec access time 4 M bit Fast SRAM Cache memory for digital camera systems.

Yoshiyuki Kawana at Sony in 1950s invented the low-collector on-resistance P+NP junction type bipolar transistor by thinning the back side of the silicon wafer, a technique now widely used for the modern backside illumination CMOS image sensors to improve sensitivity. Toshio Kato at Sony in early 1960 invented the silicon surface light etching technique and new SiO2 passivation technique for the P+NP junction type bipolar transistor with the MESA like isolation, which is now known as the shallow trench isolation with the excellent side wall SiO2 to reduce the device leakage current.

Both ideas of Yoshiyuki Kawana and Toshio Kato helped Hagiwara to form in 1975 the concept of the pinned PNP double junction type dynamic photo transistor and the Pinned PNPN triple junction type dynamic photo thyristor. The double and triple junction type dynamic photo sensor structures proposed by Hagiwara in 1975 have also the bonus features of the VOD function. Hamazaki Chip-Design Team and Kambe CCD-Process Team at Sony in 1987 developed the PPD with the built-in VOD function, capable of the electrical shutter and snap-shot picture functions with completely mechanical free parts for the first time in the world. And the last but not the least feature of the Global Shutter Function of MOS capacitor type in pixel buffer memory became now a reality by the young generation of Sony engineers after the 45 years of Hagiwara 1975 invention.

Dr. Sei-ichi Watanabe, Yoshiyuki Kawana and Toshio Kato guided Hagiwara always when in need. The author received many hints from the SONY bipolar process and device technology, which guided Hagiwara to the original 1975 invention and the 1978 successful development for the P+PNP double junction type Pinned Photodiode.

The author expresses sincere gratitude to Dr. Tsugio Makimoto, Ki-ichiro Mukai, Terushi Shimizu, Yasuhiro Ueda, Tadakuni Narabu and many fellow engineers in Sony who helped me to prepare this paper thru many fruitful discussions. They are my dear friends and mentors in private and public life.

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