

Characterization and Modeling of a Highly Reliable ONO Antifuse for High-Performance FPGA and PROM

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Abstract: The characteristics and reliability of ONO (oxide-nitride-oxide) anti-fuse devices prepared basing on 0.6μm SOI CMOS process have been studied experimentally and theoretically. The intrinsic principles of ONO dielectric breakdown were investigated with tunneling and emission models. It has been found that the conduction mechanisms of ONO dielectrics under high electric field ($>10\text{MV/cm}$) mainly obeys Fowler-Nordheim (F-N) tunneling and Poole-Frenkel (P-F) emission and Ohmic transport models. Meanwhile, the nitrogen depth distribution and the composition of the ONO stack films have been accurately determined using SIMS and EDX, respectively. The results indicate that the nitrogen concentration of interface between tunneling oxide and N⁺ sub-silicon is higher than that of interface between top oxide and N⁺ poly-silicon, which can contribute to prove the difference of top and bottom electrode interface barriers according to energy band diagrams of ONO anti-fuse devices. Besides, it is also found that the average breakdown voltage of ONO anti-fuse arrays and that of distribution decrease with increasing the number of anti-fuse cells, and the result is attributed to traps density of various areas. Moreover, the programming resistance of ONO anti-fuse cells and programming circuits decreases with increasing programming current, and the programming resistance of ONO anti-fuse cells can reach less than 200 ohm/cont when programming current is above 5mA. And the life of unprogrammed ONO anti-fuse devices can reach more than 40 years under an electric stress of 5.5v at the temperature from 25°C to 125°C. So, it can be concluded that the characteristics and reliability of the proposed ONO anti-fuse elements are suitable for applications in FPGA and PROM.

Keywords: Antifuse, Oxide-Nitride-Oxide, Breakdown Voltage, Programming Resistance, SOI

1. Introduction

Over the past years, due to the ONO anti-fuse devices exhibiting great difference in impedance before and after programming, the anti-fuse processing technology has attracted significant attention of IC designers and manufacturers, and is widely used in the area of nonvolatile memories or programmable array logic devices for radiation-hardened space environment, such as PROM, PAL, FPGA (field programmable gate arrays), and so on [1-6]. The composition, structure, electrical characteristics and reliability

of ONO antifuses have been widely studied. The ONO dielectrics layer lies between a poly-silicon conductor and a heavily doped N⁺ diffusion region of the base silicon wafer. Prior to programming, the anti-fuse cell tends to exhibit very high resistance (typically $>1\text{M}\Omega$), and the impedance may be reduced to below 1000Ω after programming under high voltage or current stress [1-4]. Under the programming voltage, the ONO sandwich melts and the base wafer grows an epitaxial “bump” into the poly-silicon in the shape of a dome. Growth of the bump shatters the ONO layer, allowing diffusion of the substrate N⁺ into the poly-silicon to form a

low-resistance path. The bump's size also makes the structure tolerant of current-induced stresses [1-4]. If anything, the high currents would increase the bump's size, strengthening the connection. Meanwhile, silicon-on-insulator (SOI) devices have superior capability in good radiation hardness, no latch-up, and high device density [7, 8]. Therefore, to realize high performance and reliability of radiation-hardened ONO anti-fuse devices for FPGA or PROM, the SOI CMOS processing technology can be applied in the ONO anti-fuse process.

In this work, the electrical properties and reliability of ONO anti-fuse devices were investigated experimentally and theoretically basing on 0.6 μm SOI CMOS process. Meanwhile, the N/O/Si depth distributions and composition of the ONO stack films have been accurately determined using SIMS and EDX, respectively. Besides, in order to characterize the electrical properties and reliability of ONO anti-fuse devices, current-voltage (I-V) and time-dependent dielectric breakdown (TDDB) were used and performed.

2. Experience

2.1. Preparation of the ONO Anti-fuse Samples

In this paper, the ONO anti-fuse samples were prepared basing on 0.6 μm SOI CMOS process (2Wells@2Polys@2Metals). The anti-fuse ONO dielectrics is formed as follows: At first, after the formation of CMOS on the SOITEC P<100> (top-Si/ bottom-oxide=1.5 μm /3.0 μm), the high density of N⁺ sub-silicon in p-well is formed by arsenic and phosphorus implantation (dose: E15) and annealing at 1050°C. Since, the tunneling oxide layer is very thin, the process of which is difficultly controlled through conventional methods. Meanwhile, in order to improve tunneling oxide/ n⁺ sub-Silicon interface properties, the oxynitridation method is taken into account. Hence, bottom oxide (i.e., tunneling oxide) is thermally grown on n⁺ sub-silicon by the low-pressure oxynitridation in mixture of N₂O and N₂ ambients (i.e., N₂O:O₂=1:5), in which the temperature and pressure are fixed at 820°C and 70 torr,

respectively [9]. And following the rich-nitrogen silicon nitride is immediately deposited by the LPCVD method. The top-oxide is formed by re-oxidation of Si_xN_y at 950°C (i.e., wet oxide). After that, a polysilicon layer is deposited and doped by phosphorus diffusion at 900°C utilizing a POCL₃ source. The ONO anti-fuse structure is illustrated as Fig. 1.

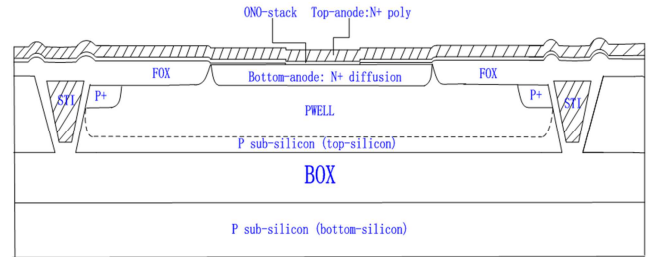


Fig. 1. Cross-sectional view of an ONO anti-fuse device basing on SOI CMOS process.

2.2. Measurement and Method

In this study, the cross-section of an ONO anti-fuse device and the composition of ONO dielectrics were measured by TEM and EDX, respectively, as shown in the fig. 2. The thickness of tunneling oxide and media Si_xN_y and top oxide are 2.9nm/4.8nm/3.0nm, respectively. Meanwhile, the nitrogen depth distribution and the composition of the films have been accurately determined using SIMS, and the depth profile of N/O/Si is shown in the fig. 3. To characterize the electrical properties of ONO anti-fuse dielectrics, capacitance-voltage (C-V) and current-voltage (I-V) measurements were carried out on MOS capacitors (i.e., N⁺ polysilicon gate / dielectrics / N-type sub-silicon). Besides, in order to characterize the electrical properties and the reliability of ONO anti-fuse devices, I-V and time-dependent dielectric breakdown (TDDB) were used and performed. I-V and high frequency (1MHz) C-V measurements were performed by HP model 4200 semiconductor parameter analyzer and HP model 4284 precision LCR meter, respectively.

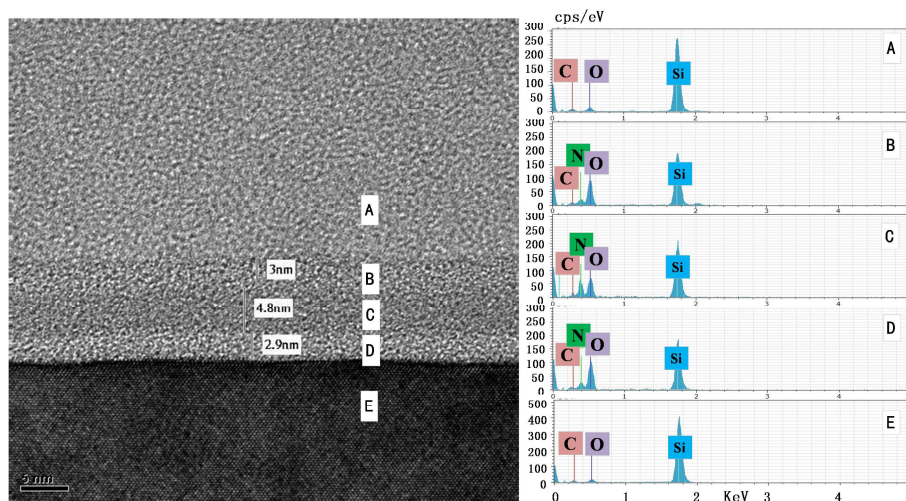


Fig. 2. TEM and EDX analysis for an ONO antifuse (A: top anode-n+polysilicon, B\C\D: ONO-stack layers, E: bottom anode).

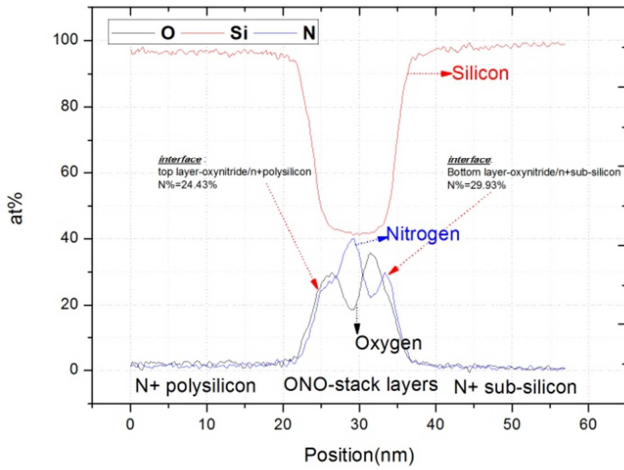


Fig. 3. SIMS depth profiles for ONO films: N, O, and Si distribution (sweeping from the top anode to the bottom anode).

3. Results and Discussion

3.1. ONO Conduction Mechanism

Fig. 4 shows I-V characteristics for ONO anti-fuse devices under different bias, and the effective electric field can be calculated approximately by V/T_{ONO} . It can be observed that the slopes of the I-V curves for ONO anti-fuse devices are approximately similar in the high-field region ($>7.5\text{MV/cm}$) with various bias. Meanwhile, the maximum breakdown fields are also similar when N+ sub-silicon and N+ poly-silicon electrodes added by +/- bias or -/+ bias, respectively. But the leakage current of low electric field is different, when N+ sub-silicon as top polarity, the leakage current in the low electric field is higher than that of N+ poly-silicon, and the difference has two to three orders of magnitude. Besides, the difference of breakdown voltage is approximately 2.5V under top and bottom electrodes with the same bias. The results can be contributed to the effect of interface roughness [10] and barrier height between cathode and ONO.

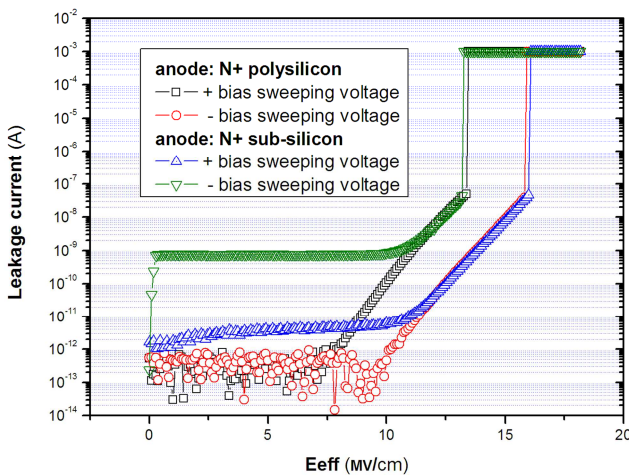


Fig. 4. I-E characteristics for the ONO structure with various bias ($E_{\text{eff}} = V/T_{\text{ONO}}$).

To study the conduction mechanism of the carriers in the ONO dielectrics, the current density (J) versus effective electric field (E_{eff}) data were fitted by Fowler-Nordheim(F-N) tunneling, ohmic transport and Poole-Frenkel(P-F) emission models, as shown in the format (1)~(5). The F-N model is based on the hot electron tunneling through a triangle-shaped energy barrier formed in the dielectric layer due to the large applied electric field. The P-F model describes the field enhanced thermal emission process of trapped electrons into the conduction band of the dielectrics [11].

$$J = AJ_1 + BJ_2 + CJ_3 \quad (1)$$

Poole-Frenkel emission model:

$$J_1 = C_1 E \exp \left\{ -q \left[\phi_B - \left(qE / \pi K_d \epsilon_0 \right)^{1/2} \right] / kT \right\} \quad (2)$$

Fowler-Nordheim tunneling model:

$$J_2 = C_2 E^2 \exp(-E_B / E) \quad (3)$$

$$E_B = \frac{4(2)^{1/2} m^* (q\phi_B)^{3/2}}{3qh} \quad (4)$$

Ohmic transport model:

$$J_3 = C_3 E \exp(-E_a/kT) \quad (5)$$

Where J is the current density, E is the applied electric field, q is the elementary charge, Φ_B is the potential barrier (in zero applied electric field) that an electron must cross to move from one atom to another in the crystal, ϵ_0 is the dynamic permittivity, d is the thickness of the insulator, K is Boltzmann's constant, K_d is dielectric constant, T is the temperature, C_1 is a function of the density of dielectrics trapping centers, C_2 is a function of the electron effective mass and the depth of the trap-potential well, C_3 is a function of the density of dielectrics trapping centers and the density of conducting carriers.

The energy band diagrams for ONO anti-fuse devices with various bias are shown in fig. 5. According to previous reports [12, 13, 14], the ONO anti-fuse conduction mechanism can be dedicated as follows.

When N+ polysilicon or N+ sub-silicon is applied with a positive bias, as shown in Fig. 5(a) and (b), holes are injected into the Si_xN_y film by direct tunneling through the reoxidized film (top-layer) or tunneling oxide (bottom-layer), and they are carried by the P-F mechanism in the Si_xN_y film (middle-layer). The holes will accumulate at the interface of the middle-layer and the bottom oxide or the middle-layer and the top-layer, although partly holes are compensated for F-N tunneling electron. Thus, such holes lead to electric field enhancement of bottom oxide (B.O) and enhance the F-N electron conduction in B.O.

However, when N+ polysilicon or N+ sub-silicon electrode is added by a negative bias, as shown in Fig. 5(c) and (d), holes are injected into the valence band of the Si_xN_y film by

the modified F-N tunneling because of the thin bottom oxide film, and they are carried by the P-F mechanism. For hole conduction from the Si_xN_y film to the electrode, two mechanisms are thought to occur: Tunneling from the trap site

of the Si_xN_y film to the electrode through the oxide and tunneling from the valence band to the electrode. The tunneling conduction from the trap site is thought to be dominant.

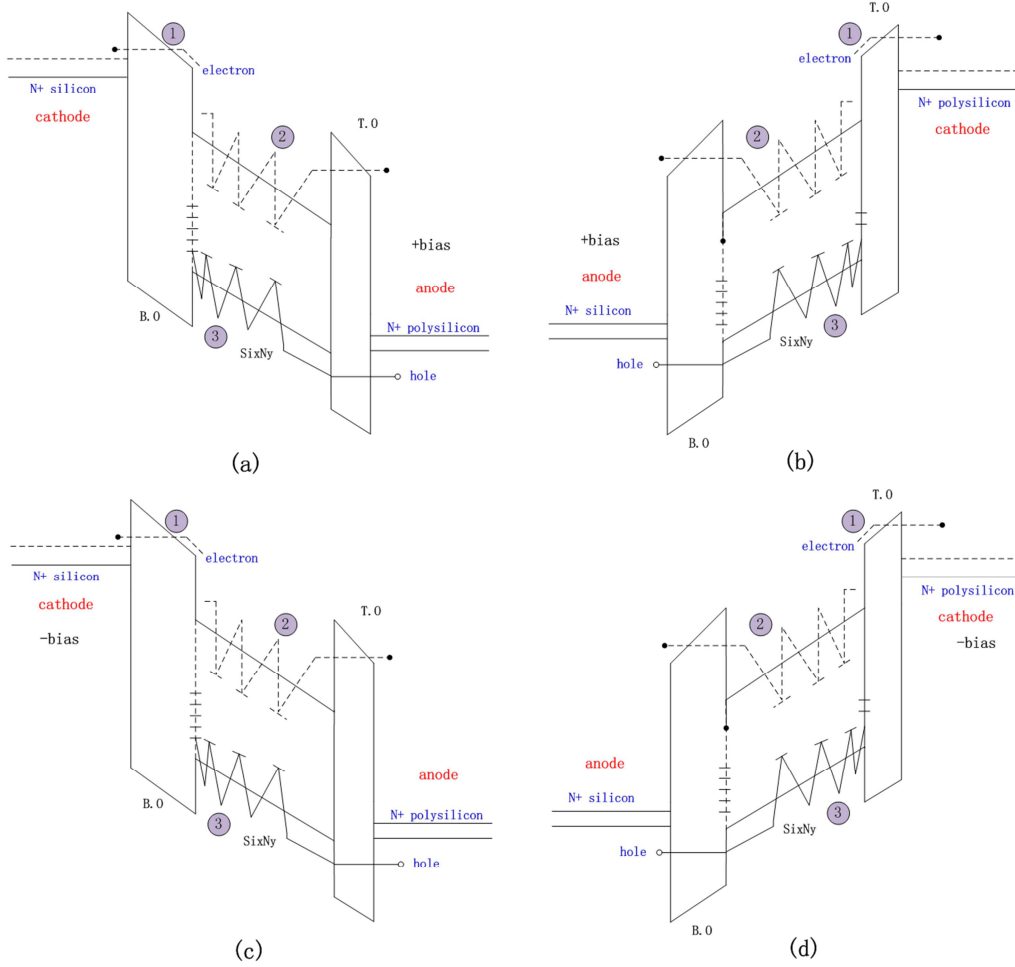


Fig. 5. The energy band diagram for ONO structure with various bias (a: N+polysilicon electrode is applied with a positive sweeping voltage; b: N+ sub-Silicon electrode is applied with a positive sweeping voltage; c: N+ sub-Silicon electrode is applied with a negative sweeping voltage; d: N+polysilicon electrode is applied with a negative sweeping voltage).

Table 1. ONO anti-fuse key stacker parameters at 25°C (a value are from Yu H.Y [6]).

ONO stacker	ΔE_c (ev)	ΔE_v (ev)	E_g (ev)
Top-layer	2.31	2.82	6.25 ^a
Middle-layer	-	-	5.8 ^a
Bottom-layer	2.79	2.84	6.75 ^a

As shown in the fig. 3, the SIMS results clearly demonstrate that the wet re-oxidation of Si_3N_4 results in a high concentration of nitrogen near ONO stack layers, and the nitrogen concentration of top-oxide and middle-oxide and tunneling oxide approximately are 24.43%, 40.15%, 29.93%, respectively. According to Yu etal [15] results of the relation between “the electron or hole barrier height and dielectric gap energy” and “the N concentration of oxynitride films”, the band gap energy of top-oxide and middle-oxide and tunneling oxide approximately are 6.75ev (ΔE_v : 3.15ev; ΔE_c : 2.45ev; ΔE_{si} : 1.12ev), 5.8ev, 6.25ev (ΔE_v : 2.95ev; ΔE_c : 2.15ev; ΔE_{si} : 1.12ev), as shown in the table 1.

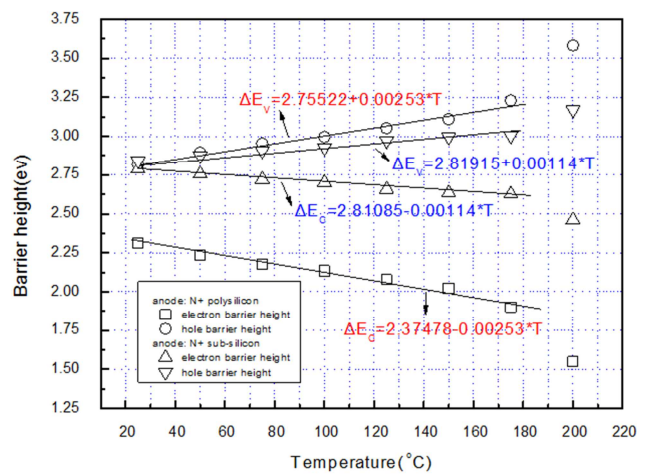


Fig. 6. The relation between interface barrier height of “tunneling oxide layer/ N+ sub-silicon” and “top layer oxide layer / N+ poly-silicon” with temperature (electron barrier height: ΔE_c ; hole barrier height: ΔE_v).

Meanwhile, the tunneling / injection properties of hot electrons (HEs) and hot holes (HHs) via the potential barrier formed by tunneling oxide or top-oxide of ONO antifuse devices are investigated. According to the principle of F-N tunneling model as shown in the format (3), the electron and hole interface barrier height of oxynitride / N+sub-silicon and oxynitride / N+ poly-silicon with various temperatures for ONO anti-fuse devices are calculated basing on the slope of J/E^2 vs $1/E$ in different bias condition, and shown in the fig. 6 and table 1, and that of ΔE_c and ΔE_v is in agreement with previous reports [15] at temperature 25°C. It can be shown that the interface barrier height of the electron and hole linearly increases or decreases with temperature from 20°C to 180°C, and the ONO breakdown voltage under different bias is strongly depended on the interface electron barrier height as shown in the fig. 7. It is understood that the decrease of ΔE_c exponentially enhances the tunneling probability of HEs, while it exponentially suppresses the tunneling probability of HHs. The positive charge(HHs) produced by injection is observed such that the cathode field for F-N current injection is enhanced and the anode field is decreased, depending on the location of these charge [10-18]. The trapped positive charges resulting from hole generation by impact ionization in the oxide lead to an increased local field and reduce barrier height of the cathode under high electric field. The P-F transport model suggests that electron trapping causes an increase in the electric field at the anode and eventually leads to breaking of Si-O bands [10-18].

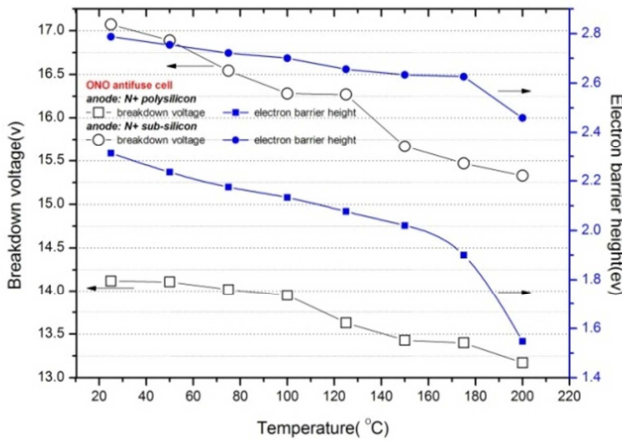


Fig. 7. ONO anti-fuse devices breakdown voltage and electron barrier height versus various temperatures from 25°C to 200°C.

Fig. 8(a) and (b) show the Poole-Frenkel(P-F) and the Fowler-Nordheim(F-N) plots of the measured current-voltage relations for the ONO antifuse devices under various bias. The plots of $\log(J/E_{eff})$ versus $E_{eff}^{1/2}$ and $\log(J/E_{eff}^2)$ versus E_{eff}^{-1} approximately behave in accordance with linear fitting, and that of adjective coefficients are more than 0.99, and which indeed indicates the exactness of the model. So the ONO conduction mechanism obeys either a P-F emission model or a F-N tunneling model. Meanwhile, the dielectric constant K_d can be extracted from slop of $\log(J/E_{eff}^2)$ versus E_{eff}^{-1} using format (2). And basing on comparing with measured K_d from

C-V characteristics of ONO anti-fuse capacitors as shown in the fig. 9 and the table 2, it is found that the matching between measured and calculated K_d is very perfect, which also prove our previous conclusion. In addition, Fig. 10 shows $\log(J/E_{eff})$ versus $1000/T$ plots for temperatures ranging from 25°C to 200°C. The temperature-dependent current at the higher electric field is mainly due to current components J_1 and J_3 . According to the P-F emission model, current density J_1 is due to field-enhanced thermal excitation of trapped electrons into the dielectric conduction band [11].

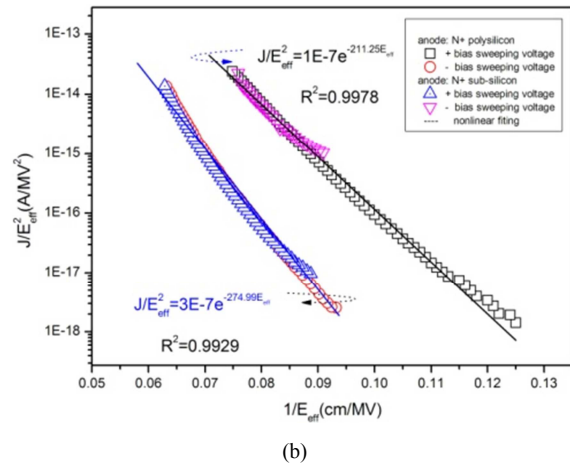
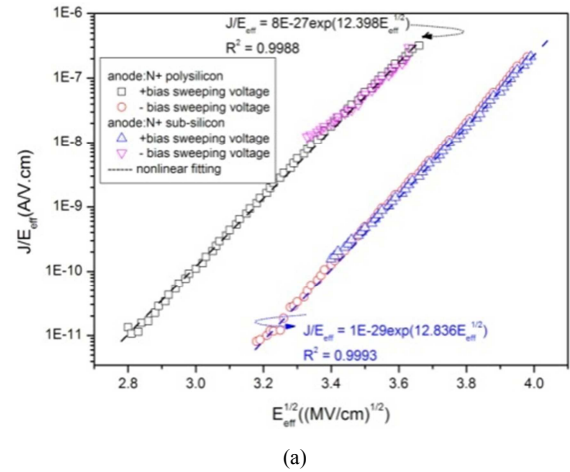


Fig. 8. Plots of (a) Poole-Frenkel: J/E_{eff} versus $E_{eff}^{1/2}$, and (b) Fowler-Nordheim: J/E_{eff}^2 versus E_{eff}^{-1} for ONO anti-fuse devices at 25°C.

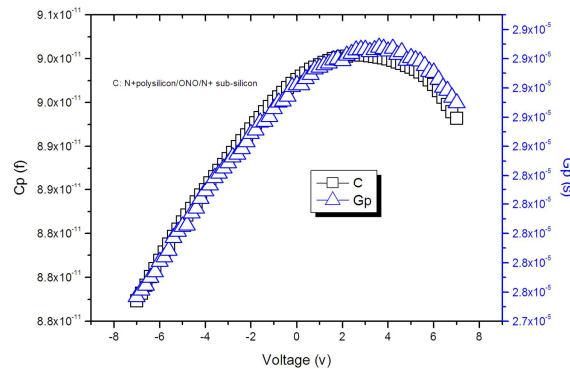
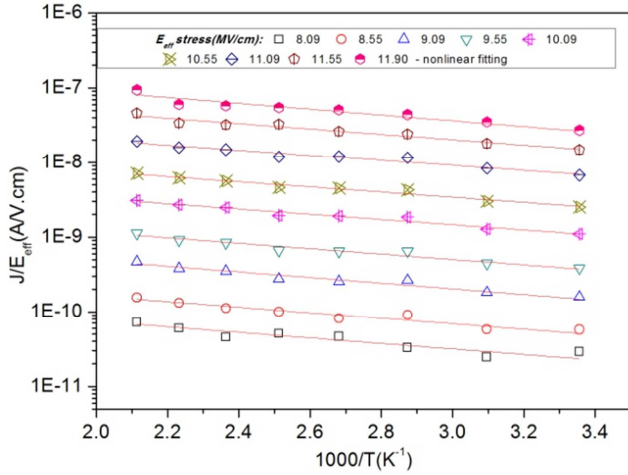


Fig. 9. C-V characteristics of ONO anti-fuse capacitors.

Table 2. Dielectric constant (Kd) extracted from different polarities as anode and C-V measured value using ONO MOS capacitors (70 μ m*300 μ m).

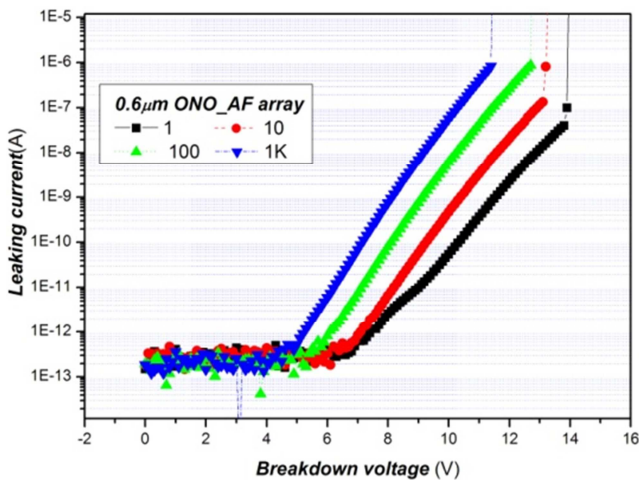
ONO stacker	Extracted from N+ polysilicon as anode under positive bias	Extracted from N+ sub-silicon as anode under positive bias	C-V measured value
Dielectric constant (Kd)	5.39	5.59	5.34

**Fig. 10.** J/E_{eff} versus $E_{eff}^{1/2}$ for an ONO antifuse at different electric field stresses and various temperatures from 25°C to 200°C.

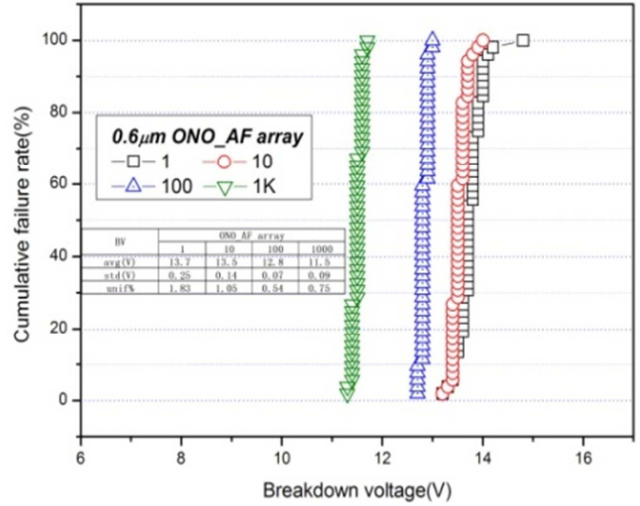
3.2. ONO Characteristics

3.2.1. Current-Voltage Characteristics

Fig. 11 shows excellent breakdown characteristics and distribution of ONO anti-fuse arrays containing anti-fuse cells from 1 to 1K. The ONO anti-fuse cells perform low leakage current under a 5.5v electric stress. Meanwhile, it is found that the average breakdown voltage of ONO anti-fuse arrays decreases with increasing the number of anti-fuse cells, and the distribution of breakdown voltage also decreases with increasing the number of anti-fuse cells by means of the uniformity and cumulative failure of BV, namely, the uniformity is defined as the std divided by the average of BV. The uniformity of arrays from 1 to 1K decreases from 1.83% down to 0.75%. The result is attributed to traps density of various areas.



(a)



(b)

Fig. 11. The breakdown voltage and distribution of ONO anti-fuse arrays at 25°C.

3.2.2. Programming Characteristics

Fig. 12 shows ONO anti-fuse programming resistance with programming time under various programming current. When programming current reaches above 0.75mA, the resistance of ONO anti-fuse cells becomes constant without changing under the increase of programming time, and that of characteristics further illustrates that the ONO anti-fuse cells have extremely short programming time (i.e., $T_{program}=307\mu$ s). Meanwhile, in order to study the relation between programming resistance with programming current of the ONO anti-fuse cells, we choose two testing structures: an ONO anti-fuse cell and two categories programming circuits, which contains an MOS transistor and an ONO anti-fuse cell (i.e., AF1+MOS) or an MOS transistor and two anti-fuse cells (i.e., AF1+AF2+MOS). The programming resistance of ONO anti-fuse cells and programming circuits decreases with increasing programming current, and the programming resistance of ONO anti-fuse cells can reach less than 200 ohm/cont when programming current is above 2mA, and that of programming characteristics is shown in the fig. 13. Besides, to further illustrate the relation of programming current and resistant, the numerical analysis for the experience date is carried out as following format (6), where the factor A and B can be extracted as 948.19 and 0.7015 basing on a power fitting model, respectively.

$$R_{pp} = A \cdot I_{pp}^{-B} \quad (6)$$

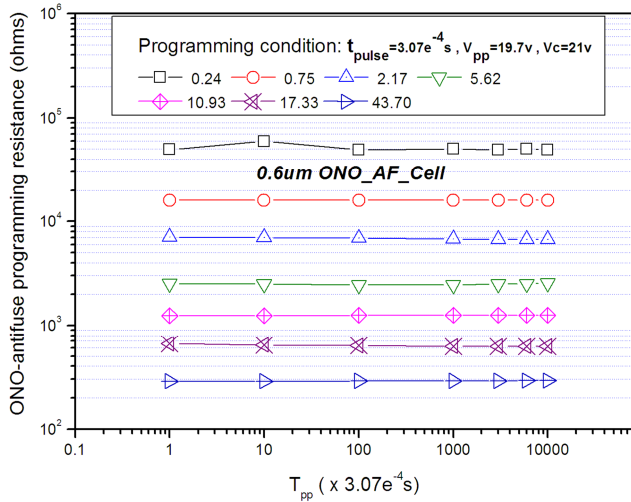
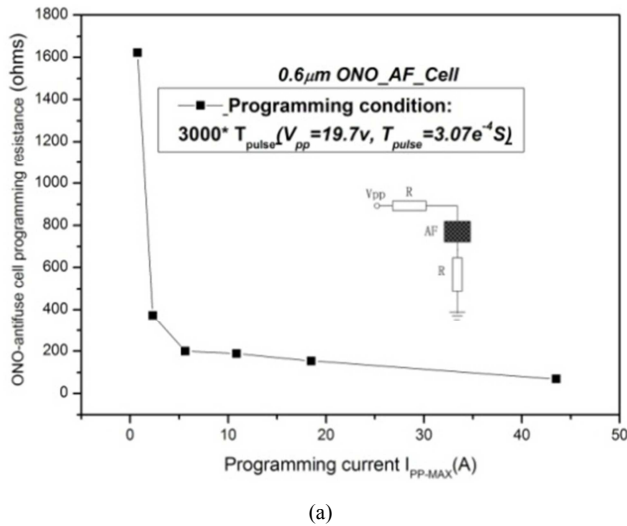
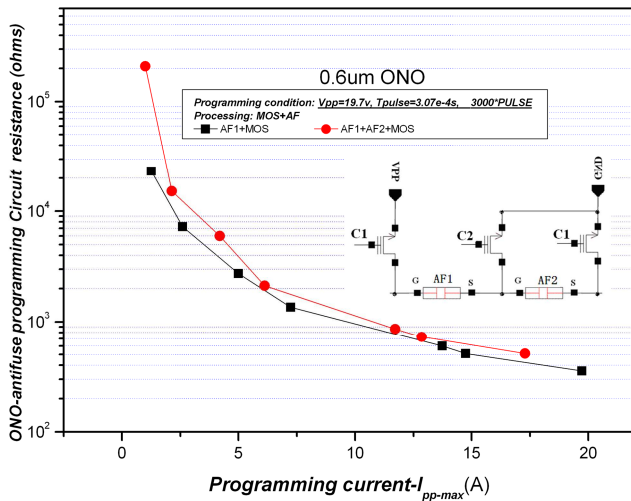


Fig. 12. ONO anti-fuse programming resistance with programming time under various programming current.



(a)



(b)

Fig. 13. ONO anti-fuse programming characteristics: (a) single anti-fuse cell; (b) programming circuits.

3.3. Time Dependent Dielectric Breakdown (TDDB)

According to ohmic transport model and I-V characteristics of ONO anti-fuse cells, the thermal active energy (E_a) of ONO dielectrics is extracted from the slope of a $\log(J/E_{eff})$ versus T^{-1} under high effective electric field (E_{eff}) using the format (2) and (5), and the E_{eff} is choose basing on electrode bias from 8MV/cm to 11MV/cm for N+ poly-silicon as anode and from 10.5MV/cm to 13MV/cm for N+ sub-silicon as anode, respectively. Meanwhile, it is also found that E_a versus E_{eff} forms a linear equation as shown in fig. 14, and the thermal active energy (E_a) of ONO dielectrics under a 5.5v electric stress condition are calculated as 0.343 and 0.349 for N+ poly-silicon and N+ sub-silicon as anode, respectively.

Besides, the results indeed indicate that the ONO antifuse devices conduction mechanism mainly obeys a P-F emission model or a F-N tunneling model or ohmic transport model. So the TDDB of ONO dielectrics should mainly be dependent on E model basing on Mc Pherson and Baglee^[18,19] thermochemical foundation, and the E model is expressed as an equation(7).

$$t_{50} = A \exp(-B \cdot E_{eff}) \cdot \exp(E_a/kT) \quad (7)$$

$$E_a = -0.04633E_{eff} + 0.57493 \quad (8)$$

Where t_{50} is the median time to breakdown, A and B are constant coefficient and field acceleration parameter, respectively. According to slops of $\log(t_{50})$ versus E_{eff} under different temperature basing on the TDDB of ONO dielectrics shown in the fig. 15, the factor A and B can be extracted by E model (i.e., the value of A and B are about $4.38E14$ and 3.3455 , respectively). So, it can be calculated that the life of an ONO anti-fuse cell ($0.6\mu m \times 0.6\mu m$) under an electric stress of 5.5v at the temperature from 25°C to 125°C is more than 40 years according to the format (7) and (8).

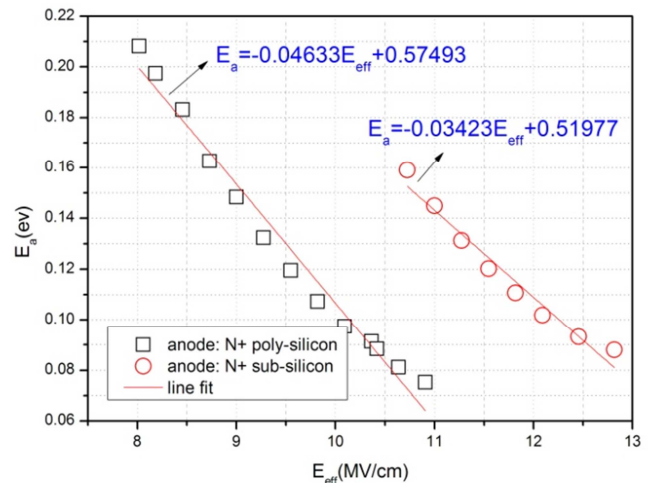


Fig. 14. Thermal active energy (E_a) versus effective electric field (E_{eff}) for an ONO antifuse at different bias.

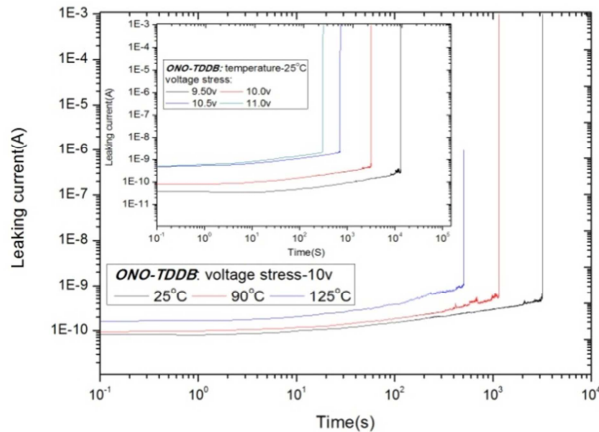


Fig. 15. TDDB of the ONO anti-fuse devices under different temperatures or electric stresses.

4. Conclusions

Highly reliable ONO anti-fuse devices ($0.6\mu\text{m} \times 0.6\mu\text{m}$) with excellent electrical characteristics, such as low programming resistance, low programming time, and good BV uniformity, can be successfully prepared basing on $0.6\mu\text{m}$ SOI CMOS process. The intrinsic principles of ONO dielectric breakdown were investigated experimentally and theoretically with tunneling and emission models. Firstly, it has been found that the conduction mechanisms of ONO dielectrics under high electric field ($>10\text{MV/cm}$) mainly obeys Fowler-Nordheim (F-N) tunneling and Poole-frenkel (P-F) emission and Ohmic transport models. Meanwhile, according to the depth profile of N/O/Si for an ONO antifuse using SIMS, the difference of top and bottom electrode interface barriers is due to the difference of nitrogen concentration at interface for “tunneling oxide /N+ sub-silicon” and “top oxide / N+ poly-silicon”. Besides, the average breakdown voltage of ONO anti-fuse arrays and that of distribution decrease with increasing the number of anti-fuse cells, and the uniformity of arrays from 1 to 1K decreases from 1.83% down to 0.75%. In addition, the programming resistance of ONO anti-fuse cells and programming circuits decreases with increasing programming current, and the programming resistance of ONO anti-fuse cells can reach less than 200 ohm/cont when programming current is above 5mA, and the programming time T_{pp} is below 3.07E-4s . Finally, it can be predicated that the life of unprogrammed ONO anti-fuse devices can reach more than 40 years under an electric stress (5.5v) at the temperature from 25°C to 125°C by means of TDDB. So, all these results strongly indicate that the characteristics and reliability of the proposed ONO anti-fuse elements are suitable for applications in nonvolatile memory devices, such as PROM, FPGA and so on.

References

- [1] S. Chiang, R. Wang, J. Chen, K. Hayes, J. McCollum, E. Hamdy, C. Hu, “Oxide-Nitride-Oxide Antifuse Reliability,” International Reliability Physics Symposium, 1990, 50(12), 186-192.
- [2] S. Chiang, R. Wang, T. Speers, J. McCollum, E. Hamdy, C. Hu, “Conductive channel in ONO formed by controlled dielectric breakdown,” International Symposium on VLSI Technology, Systems, and Applications, 1992, 20-21.
- [3] J. Chen, S. Eltoukhy, S. Yen, R. Wang, F. Issaq, G. Bakker, J. L. Yeh, E. Poon, D. Liu and E. Hamdy, “A modular $0.8\mu\text{m}$ technology for high performance dielectric antifuse field programmable gate arrays,” International Symposium on VLSI Technology, Systems, and Applications, 1993, 160-164.
- [4] A. Iranmanesh, Y. Karpovich, S. Yoon, “Antifuse reliability and link formation models,” International Integrated Reliability Workshop, 1994, 90-94.
- [5] M. M. Amr, Z. H. Esmat, L. M. John, “Programmable Low Impedance Anti-fuse Element,” U.S. Pat. No. 4943538, 1990.
- [6] L. M. John, “Method of forming an antifuse element with substantially reduced capacitance using the locos technique,” U.S. Pat. No. 5057451, 1991.
- [7] B. K. James, L. Shih-Chia, “Low-voltage SOI CMOS VLSI Devices and Circuits,” John Wiley & Sons, Inc., New York, 2001, 1-7.
- [8] J. R. Schwank, V. Ferlet-Cavrois, M. R. Shaneyfelt, P. Paillet, P. E. Dodd, “Radiation Effects in SOI Technologies,” IEEE TRANSACTIONS ON NUCLEAR SCIENCE, 2003, 50(3), 522-528.
- [9] G. Z. Liu, G. S. Hong, R. C. Zheng, X. D. Wu, and W. J. Yang, “High Quality of Ultra-Thin SiO_xN_y Films Prepared in Nitrous Oxide Ambients Using Thermal Low-Pressure Oxynitridation,” Materials and Manufacturing Processes, 2014, 29(9), 1050-1055.
- [10] N. Matsuo, H. Fujiwara, and T. Koyanagi, “Numerical analysis for conduction mechanism of thin oxide-nitride-oxide films formed on rough poly-Si,” IEEE ELECTRON DEVICE LETTERS, 1996, 17(2), 56-58.
- [11] S. S. Gong, M. E. Burnham, N. D. Theodore, and D. K. Schroder, “Evaluation of Qbd for Electrons Tunneling from the Si/SiO₂ Interface Compared to Electron Tunneling from the Poly-Si/SiO₂ Interface,” IEEE TRANSACTIONS ON ELECTRON DEVICES, 1993, 40(7), 1251-1257.
- [12] S. Mori, E. Sakagami, H. Araki, Y. Kaneko, K. Narita, Y. Ohshima, N. Arai, and K. Yoshikawa, “ONO Inter-Poly Dielectric Scaling for Nonvolatile Memory Applications,” IEEE TRANSACTIONS ON ELECTRON DEVICES, 1991, 38(2), 386-391.
- [13] Z. H. Liu, P. T. Lai, Y. C. Cheng, “Characterization of Charge Trapping and High-Field Endurance for 15-nm Thermally Nitrided Oxides,” IEEE TRANSACTIONS ON ELECTRON DEVICES, 1991, 38(2), 344-354.
- [14] N. Matsuo, A. Sasaki, “Electrical Characteristics of Oxide-Nitride-Oxide Films Formed on Tunnel-Structured Stacked Capacitors,” IEEE TRANSACTIONS ON ELECTRON DEVICES, 1995, 42 (1), 1340-1343.
- [15] H. Yu, Y. T. Hou, M. F. Li, D. L. Kwong, “Investigation of Hole-Tunneling Current Through Ultrathin Oxynitride/Oxide Stack Gate Dielectrics in p-MOSFETs,” IEEE TRANSACTIONS ON ELECTRON DEVICES, 2002, 49 (7), 1158-1164.
- [16] M. Wang, J. Huang, A. Anopchenko, D. Li, D. Yang, L. Pavesi, “Light emission properties and mechanism of low-temperature prepared amorphous Si_3N_4 films. II. Defect states electroluminescence,” JOURNAL OF APPLIED PHYSICS, 2008, 104(8), 083505-083505-4.

- [17] Y. Y. Chiu, B. J. Yang, F. H. Li, R. W. Chang, W. T. Sun, et al, "Characterization of the charge trapping properties in p-channel silicon-oxide-nitride-oxide-silicon memory devices including SiO," Japanese Journal of Applied Physics, 2015, 54(10), 181-184
- [18] J. W. McPherson, D. A. Baglee, "Acceleration factors for thin gate oxide stressing," Microelectronics Reliability, 1986, 26(4), 796-800.
- [19] J. W. McPherson, D. A. Baglee, "Acceleration factors for thin oxide breakdown," J. Electrochem. Soc., 1985, 132(8), 1903-1908.