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# Effect of phase transition temperature of $\text{BaTi}_{0.9}\text{Sn}_{0.1}\text{O}_3$ on the operating mode of ferroelectric random access memories (FeRAM)

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**Abstract:** The outstanding dielectric, ferroelectric and piezoelectric properties of  $\text{BaTiO}_3$  make it the desirable primary material for a variety of applications such as nonvolatile memories (RAM). At the Curie's temperature the dielectric properties of  $\text{BaTiO}_3$  undergo phase transition. The Landau-Devonshire's phenomenological theory has been investigated in this paper to present the relation between the temperature and the electric induction. The effect of the variation of electric induction versus temperature of  $\text{BaTi}_{0.9}\text{Sn}_{0.1}\text{O}_3$  investigated in the fabrication of nonvolatile ferroelectric random access memories (FeRAM) which may lead us to discover a strange phenomenon called «determinist chaos », now the FeRAM lose its reliability.

**Keywords:** Ferroelectric Capacitor, FEM-FET Transistor, FeRAM, Landau-Devonshire's Theory of Phase Transition, Ferroelectric Properties

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## 1. Introduction

L'électronique moderne nécessite la présence d'appareillages dans des volumes de plus en plus restreints, une course est engagée pour essayer de réduire au maximum la taille des FeRAM, tout d'abord ca a commencé par la réduction de la taille des transistors et des condensateurs, mais ce la se traduit par l'apparition d'un courant de fuite important, pour palier à ce problème, on envisage d'introduire des matériaux diélectrique dans la construction des composantes électroniques afin d'augmenter l'efficacité des FeRAM. Ferroelectric random access memories have attracted much attention because of the lower writing voltage and faster switching speed than those of Flash memory [1,2,20]. Among them,  $\text{PbZr}_x\text{Ti}_{1-x}\text{O}_3$  (PZT) thin films have been extensively investigated, since PZT exhibits several advantages, such as a relatively low processing temperature. However, PZT exhibits a serious disadvantage in switching endurance with common Pt electrodes [3-4]. Although fatigue resistance of PZT has been improved with oxide electrodes, usage of oxide electrode increases complexity of fabrication process and cost

[4,21,22]. Furthermore, PZT contains an environmentally hazardous element, Pb. So, environmentally safe alternative ferroelectric materials have been investigated for memory applications.  $\text{SrBi}_2\text{Ta}_2\text{O}_9$  (SBT) and  $\text{Bi}_4\text{Ti}_3\text{O}_{12}$  (BIT), among lead-free ferroelectric, are promising materials for these purposes and have been extensively studied [5,6-9]. SBT thin films show superior fatigue endurance against polarization switching, but it has a disadvantages, such as high process temperature of 750-850°C. Therefore, we can replace the (SBT) and (BIT) by another ferroelectric material, as  $\text{BaTiO}_3$  (BTS), which have a low process temperature, a large remanent polarization and higher dielectric permittivity. Furthermore  $\text{BaTiO}_3$  has the highest dielectric constant  $\approx 10^4$  at the phase transition temperature (Curie temperature,  $T_c=120^\circ\text{C}$ ), while at room temperature the dielectric constant decreases to  $1/5 \cdot 10^4$ , which greatly limits its applications, and causes a big problem because in practice it is not possible to program the memory tricks to  $120^\circ\text{C}$ . It is supposed that theoretically the Curie point of  $\text{BaTiO}_3$  may be lowered and broadened when the active ions  $\text{Ti}^{4+}$  are partially replaced by the non-active  $\text{Sn}^{4+}$  or  $\text{Zn}^{4+}$  [10]. Then a new method (low temperature solid-state

reaction) proposed by Shi-Wen and al. [11], has been exploited to synthesize BaTiO<sub>3</sub>. This method has many advantages, no solvents, no pollution and high yield. So the new material BaTiO<sub>3</sub> doped by Sn (BaTi<sub>0.9</sub>Sn<sub>0.1</sub>O<sub>3</sub>), synthesized by low temperature Solid-State reaction [11], show excellent dielectric properties. This method not only improved dielectric constants but also reduced dielectric loss, and lowered phase transition temperature to 23,5°C, without changing the Landau's parameters[11].

L'objectif principale de ce travail, fût l'étude de l'influence de la température sur le comportement de la FeRAM, par effet de transition de phase subit par le diélectrique avec le quel le transistor et le condensateur sont constitués, tout on se basons sur la théorie de transition de phase de Landau. In this paper we present the temperature effect of BTS on the operating mode of FeRAM. We also rely on the Landau-Devonshire's theory of phase transition, which used in recent previous work by Ourrad et al. [12], and Benouaz and al [13]. We have proposed a numerical simulation for modeling the behavior of the electric induction of BaTi<sub>0.9</sub>Sn<sub>0.1</sub>O<sub>3</sub> under temperature effect, below and above the Curie's temperature. However, the modeling and the simulation are concerned in particular the FeRAM, the ferroelectric capacitor and transistor. -Les circuits intégrés contenant les FeRAM sont des circuit électroniques de type non linéaire et peuvent être modélisées par des équations différentielles ordinaires, l'étude de ce type d'équations peut nous amener à la découverte du phénomène étrange appelé « chaos ». Integrated circuits containing FeRAM are non-linear circuit's type and can be modeled by ordinary differential equations. The study of such equations may lead us to discover the strange phenomenon called "chaos", since the oscillating electric induction over the same frequency as the external field applied to FeRAM.

## 2. Theoretical Model

### 2.1. FeRAM 's Structure

The figure 1 shows a schematic drawing of the FeRAM structure [14]. The unit cell was formed by one transistor and one ferroelectric capacitor which were connected in parallel, during the operation, one capacitor was selected randomly by cutting off it's pare transistor. Controlling the voltage across the capacitor is provided by three conductive lines called "bit line", "word line", "plate line".

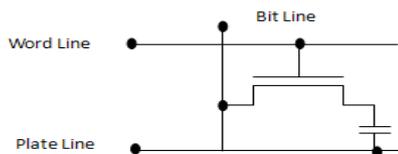


Fig. 1. Standard structure 1T/1C, (1 transistor (T) for 1 capacitor (C)).

### 2.2. Basic Hypothesis of BaTiO<sub>3</sub> Ferroelectric Material

In a phenomenological description of the ferroelectric

phase transitions in BaTiO<sub>3</sub> L'énergie libre d'un matériau diélectrique peut se développer en fonction de la polarisation sous la forme de l'équation (1); the spontaneous polarization is

$$P = (P_1, P_2, P_3)$$

and is chosen as the order parameter [15]. In the order to describable the three ferroelectric transitions in a BaTiO<sub>3</sub> single crystal, i.e. from paraelectric cubic to ferroelectric tetragonal, orthorhombic and rhombohedral. We expressed the Landau-Devonshire's free energy of a tetragonal c-domain with ,  $P=(0,0,P_3)$  by the following relation

$$G = (\alpha_1 + \beta_3)P_3^2 + (\alpha_{11} + \beta_{33})P_3^4 \quad (1)$$

Where  $\alpha_1, \alpha_{11}, \beta_3, \beta_{33}$  represent Landau's coefficients and G is the free energy of BaTiO<sub>3</sub>. The value of the polarization at thermal equilibrium is obtained by minimizing the free energy with respect to P [16]. Thus spontaneous polarization in an electric field is obtained by deriving G with respect to P, as:

$$P_s = \pm \sqrt{\frac{-(\alpha_1 + \beta_3)}{2(\alpha_{11} + \beta_{33})}} \quad (2)$$

According to the thermodynamics of dielectrics [17], the electric field in a dielectric is written as:

$$E = \left( \frac{dG}{dP} \right) \quad (3)$$

Knowing that the electric polarization P is the electric induction D (electric displacement Charges), then the electric field takes the following form:

$$E = 2(\alpha_1 + \beta_3)D + 4(\alpha_{11} + \beta_{33})D^3 \quad (4)$$

On the other hand, the dielectric permittivity expressing the property of the material to oppose the passage of electric current [18], is given by:

$$\epsilon = \frac{dD}{dE} \quad (5)$$

Where  $\epsilon$  is the dielectric permittivity, D is the dielectric induction and E is the electric field. From equations (4) and (5), we obtain the relation which rely the dielectric permittivity  $\epsilon$  to the macroscopic displacement, as:

$$\frac{1}{\epsilon} = 2(\alpha_1 + \beta_3) + 12(\alpha_{11} + \beta_{33})D^2 \quad (6)$$

Where  $\alpha_1 = \alpha_0(T - T_c)$  and  $\alpha_0 = \frac{1}{2\epsilon_0 C}$ ,

$\epsilon_0$  is the permittivity of the vacuum, C is the Curie

–Weiss constant.

The variation of dielectric permittivity with the electric flux is nonlinear, and is given by the following relationship:

$$\varepsilon^{-1} = 2(\alpha_0(T - T_c) + \beta_3) + 12(\alpha_{11} + \beta_{33})D^2 \quad (7)$$

This dielectric permittivity of BST can permit to explain the FeRAM phase transition phenomenon.

### 3. Modeling of FeRAM

FeRAM memory chosen in our study is the combination of 1T/1C, and to increase memories performance, our proposition is to place the (BTS) ferroelectric layer under the transistor oxide layer, and between the anode and the cathode of capacitor, so we obtain a new combination of FeRAM, which is (1FeFET/1 FeCAP). For this study, we propose two mathematical models:

The first model represents the behavior of the ferroelectric capacitor (FeCAP) versus temperature and voltage,

The second model is reserved to transistor ferroelectric (FeFET).

#### 3.1. Modeling of Ferroelectric Capacitor

To increase the performance of capacitor, we propose to introduce a ferroelectric material BaTi<sub>0.9</sub>Sn<sub>0.1</sub>O<sub>3</sub> (BTS) between the anode and the cathode of capacitor, its capacity takes the following form:

$$C = \frac{\varepsilon S}{e} \quad (8)$$

Where  $e$  is the thickness of capacitor and  $S$  is the surface of the electrode of capacitor. Applying a voltage on the FeRAM, leads to the reorientation of dipole moments of the BaTi<sub>0.9</sub>Sn<sub>0.1</sub>O<sub>3</sub> ferroelectric material according to the following relation:

$$D = \varepsilon_0 E + P = \varepsilon E \quad (9)$$

And  $Q = D.S$

By injecting equation (7) into (8), we obtain

$$C = \frac{S}{e(2(\alpha_0(T - T_c) + \beta_3) + 12(\alpha_{11} + \beta_{33})D^2)} \quad (10)$$

It is clear in equation (10) that when we introduce the ferroelectric in the capacitor, the ability of the ferroelectric capacitor varies in a non-linear with temperature and applied voltage, hence the nonlinearity of the electronic circuit.

Moreover, to assess the behavior of ferroelectric capacitor, we can connect it in series with a resistance, because it approaches to reality.

The application of Kirchhoff's laws yields the relation:

$$RI + \frac{Q}{C} = Ue^{(i\omega t)} \quad (11)$$

$$\text{With } I = \frac{dQ}{dt}$$

Where  $R$  is the resistance (Ohms),  $\omega$  is the pulsation and  $t$  is the time. Then the equation (11) can be expressed as:

$$\frac{dD}{dt} + \frac{eA}{RS}D + \frac{eB}{RS}D^3 = \frac{U}{RS}e^{(i\omega t)} \quad (12)$$

With

$$A = 2\alpha_0(T - T_c) + \beta_3$$

$$B = 12(\alpha_{11} + \beta_{33})$$

**Modeling of Ferroelectric Transistor** The transistor chosen in our study is FeFET, where investigated by BaTi<sub>0.9</sub>Sn<sub>0.1</sub>O<sub>3</sub> ferroelectric interface layer, because the continual reduction of transistor dimensions MOS structures, and capacitor is now leading the industry microelectronics to meet a great technological challenge. Indeed, involving thicknesses increasingly low, this size reduction is the cause of leakage currents excessive tunneling, so the solution proposed to remedy this problem is the replacement of the silica (SiO<sub>2</sub>) of transistor by an oxide of higher dielectric permittivity as BTS [18].

We applied to the FeRam an alternative voltage of the following form:

$$U = U_0 e^{(i\omega t)}, \quad \omega = 2\pi f \quad (13)$$

$U_0$  is the amplitude of applied voltage. Then the voltage of the transistor can be expressed as:

$$U_{DS} = \frac{I_{DS} \cdot T_{ox} \cdot L}{\mu^* \varepsilon \varepsilon_0 (U_{GS} - U_{th}) Z} \quad (14)$$

Where

$\mu^*$  is the mobility of the charge in the Channel of transistor

$U_{DS}$  is the tension between the drain and the source of the transistor

$U_{GS}$  is the tension between the grille and the source of the transistor

$I_{DS}$  is the intensity between drain terminal and source

$T_{ox}$  is thickness of the gate oxide

$L$  is width of the MOS transistor

$Z$  is the width of the grid

The injection of equation (7) into equation (14) yields:

$$U_{DS} = \frac{T_{ox} \cdot L \cdot S}{\mu^* \varepsilon_0 (U_{GS} - U_{th}) Z} (A + BD^2) \frac{dD}{dt} \quad (15)$$

Since the capacitor is connected in parallel with transis-

tor, then we can deduce that:

$$U_{DS} = \frac{Q}{C} = U_0 e^{(i\alpha t)} \quad (16)$$

From equation (16), we obtain the relationship of the temporal variation of the electric induction:

$$\frac{dD}{dt} = \frac{\mu^* \epsilon_0 (U_{GS} - U_{th}) Z U_0 e^{(i\alpha t)}}{T_{ox} \cdot L \cdot S (A + BD^2)} \quad (17)$$

The equation (17) has the form of an ordinary differential equation, where the electric flux varies in a non-linear function of temperature respect to time. It is clear that the ferroelectric  $\text{BaTi}_{0.9}\text{Sn}_{0.1}\text{O}_3$  produce a non-linearity in the behavior of FeRAM.

## 4. Numerical Simulation and Results

For numerically solve our differential equations, we use the forth-order Runge-Kutta method and Landau's parameters of BTS. The physical parameters of BTS used in this study are summarized in table 1 [11,12,15,16].

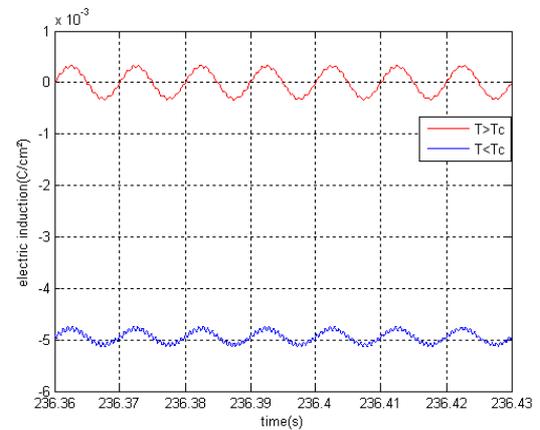
**Table 1.** Used physical parameters for  $\text{BaTi}_{0.9}\text{Sn}_{0.1}\text{O}_3$ .

Parameters	Values
$\alpha_0$	$0,041 \cdot 10^7 \text{ Nm}^6/\text{C}^4$
$\beta_3$	$1,923 \cdot 10^{12} \text{ Nm}^6/\text{C}^4$
$\alpha_{11}$	$12403,65 \cdot 10^7 \text{ Nm}^6/\text{C}^4$
$\beta_{33}$	$4,8 \cdot 10^8 \text{ Nm}^6/\text{C}^4$
$\epsilon_0$	$8,85 \cdot 10^{-12} \text{ F/m}$
$R$	$2 \text{ m}\Omega$
$U_{GS} - U_{th}$	$4 \text{ V}$
$\mu^*$	$675 \text{ (cm}^2/\text{V} \cdot \text{s.)}$
$T_{ox}$	$40 \cdot 10^{-9} \text{ m}$
$S$	$0.4 \text{ mm}$
$L$	$2 \cdot 10^{-6} \text{ m}$
$Z$	$3 \cdot 10^{-6} \text{ m}$

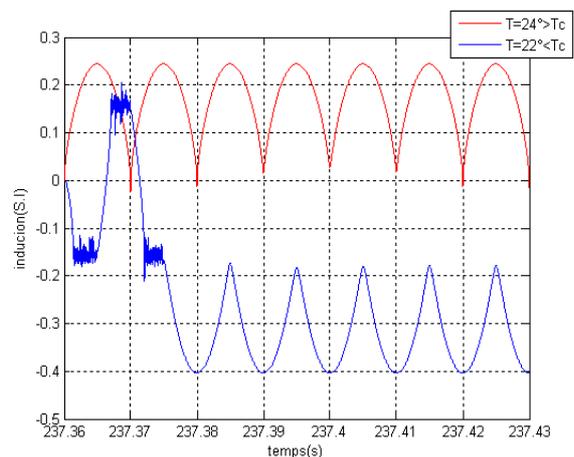
Firstly, we plot the variation of the electric induction versus time with the temperature below and above the Curie's Temperature, of the ferroelectric capacitor defined by equation (12). According to figure 2, we see that there's

a good agreement with the Landau's theory [20], so in fact for a temperature  $T=22^\circ\text{C} < T_c$ , the electric induction oscillates towers nonzero, this means in practical terms, that the dipole moment in this phase ferroelectric exist, and can be change its direction under the effect of applying electric field. But at a temperature  $T=24^\circ\text{C} > T_c$ , the induction oscillates around a zero value, it means the non existence of the electric induction, the capacitor is discharged.

Secondly, we plot the variation of the electric induction of the transistor, while we rely on equation (17). It is clear from fig. 3 that the phase transition temperature influence on the electric induction, since the value of the electric induction change. It goes from a positive value for  $T > T_c$  to a negative value for  $T < T_c$ , thus the principle of writing and reading of the FeRAM binary data "1" and "0" must be verified because the hysteresis loop of this memory will undergo a change in the remanent polarization.



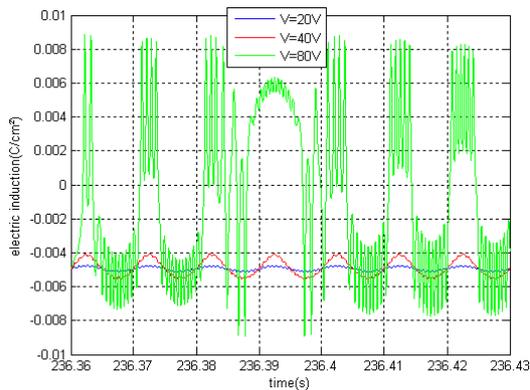
**Fig. 2.** Variation of the induction for  $T < T_c$  and  $T > T_c$  with respect to time.



**Fig. 3.** Variation of the induction with time for two phases temperature.

Thirdly, we plot the variation of the electric induction of FeRAM according to the applied voltage. Figure 4 illustrate the birth of a strange and unexpected phenomenon in more increases the value of the applied voltage, the so-called chaotic behavior. But if we observe well this figure, we note that this behavior is not really chaotic, because at a certain speed, this is called deterministic

chaos.



**Fig. 4.** Variation of the electric induction versus time for several voltages.

## 5. Conclusion

The introduction of the ferroelectric material " $\text{BaTi}_{0.9}\text{Sn}_{0.1}\text{O}_3$ " intended to increase the capacity of capacitor and transistor and our numerical simulation have shown that we can program the FeRAM only below the  $T_c$  temperature since in the opposite case the induction oscillates around the zero value and led to the failure because we must find a thermal check solution for avoid the electric induction chaotic behavior. These results may provide some insight into the design and performance of FeRAM.

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