



# An Ultra-Low-Power 5 GHz LNA Design with Precise Calculation

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**Abstract:** In this paper, an ultra-low-power low-noise amplifier (LNA) at 5GHz is proposed. The main focus is on precise computation of output impedance, input impedance, and gain of the LNA. The LNA is composed of a common-source LNA and a cascode LNA. In fact, the cascode LNA can assist to have more stability by declining S12 considerably. Plus, it can be beneficial via increasing the gain of the second stage of the final LNA. In addition, in order to emphasize the significance of the meticulous calculations, the formulas calculated in this paper are compared with their counterparts in other papers. The combination of two different supply voltage is mentioned as an approach to bring down the power dissipation of the circuit. Simulation is performed by MATLAB, HSPICE, and Advanced Design System (ADS). TSMC 0.18 um CMOS process is used to evaluate the circuit. The LNA is analyzed with two different voltage supply 0.7 V and 0.9 V. The input matching (S11) is -14 dB and -16 dB for voltage supply 0.7 V and 0.9 V respectively. Plus, power dissipation, noise figure (NF), and gain (S21) are 532  $\mu$ W, 944  $\mu$ W, 1.25 dB, 1.05dB, 15dB, and 17dB for voltage supply 0.7 V and 0.9 V respectively.

**Keywords:** Cascode, Common Source, Precise Calculation, Ultra-Low-Power, Low Noise

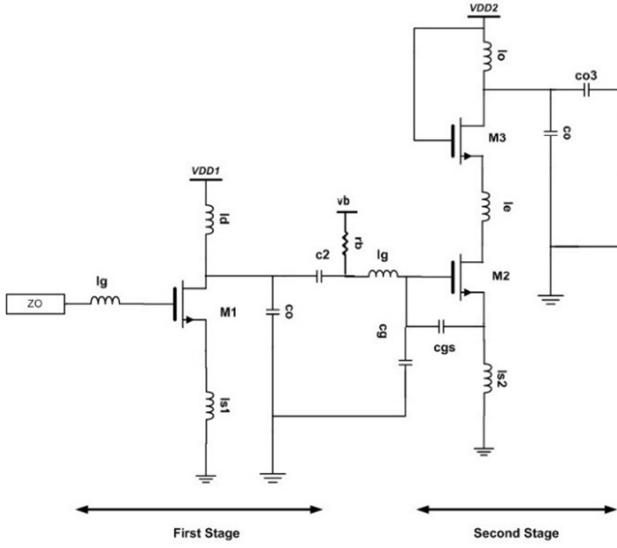
## 1. Introduction

RF receivers are composed of three integral elements, including Mixer, Oscillator, and Low Noise Amplifier (LNA). In fact, the main purpose of utilizing LNA is that the signal is amplified with the lowest possible noise. The performance of an LNA can be evaluated by Noise Figure (NF), Scattering parameters or S-parameters, third order intercept point (IIP3), and power dissipation (Pdiss). Each of the aforementioned factors is to justify a specific task of an LNA. Indeed, the performance of an LNA against noise can be interpreted by NF. Plus, stability, impedance matching, and gain have been analysed by S-parameters. In addition, IIP3 represents the linearity of the circuit, and voltage supply, the size of transistors, and power dissipation are interdependent. Furthermore, different factors such as topology, technology, and bandwidth have been focused widely. Different topologies consisting of cascode, cascade, and differential have been used and considerable results have been achieved [1-6]. An LNA can be designed to operate at a particular frequency, which is called narrow-band, or to perform during a series of frequencies, which is called

wideband [7-10]. The technology has been brought down constantly from micrometres to nanometre. In this paper, an LNA is designed with precise calculation of input and output impedance and gain with the intention of the lowest possible power dissipation.

## 2. Proposed LNA

The design of an LNA can be carried out by the size of transistors, s-parameters, voltage source, inductors, capacitors, and resistors within the circuit. In other words, voltage source and width of transistors define the bias of the circuit, specifying power dissipation. The scattering parameters are calculated by input and output impedance of an LNA and elements connected to its terminals. Hence, miscalculations in input impedance, output impedance, equivalent circuit, and the gain might exacerbate the ultimate results. Therefore, the more precise calculations and equivalent circuits are, the more reliable their results will be. The proposed LNA is composed of two stages, including a common-source (CS) LNA and a cascode LNA, demonstrated in figure 1.

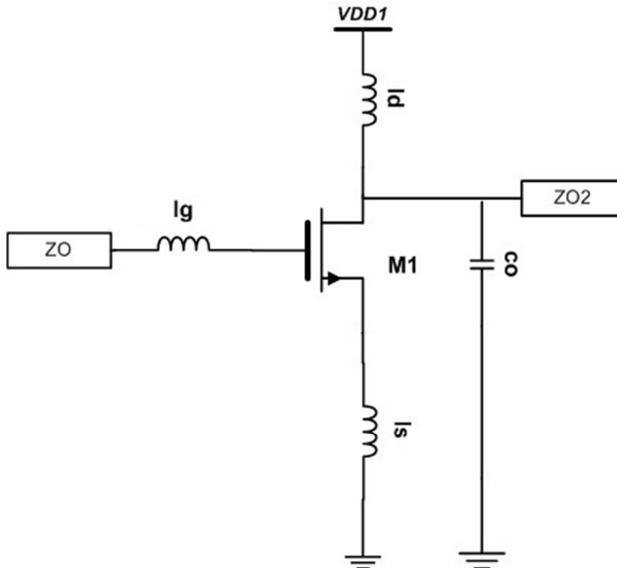


**Figure 1.** The proposed LNA.

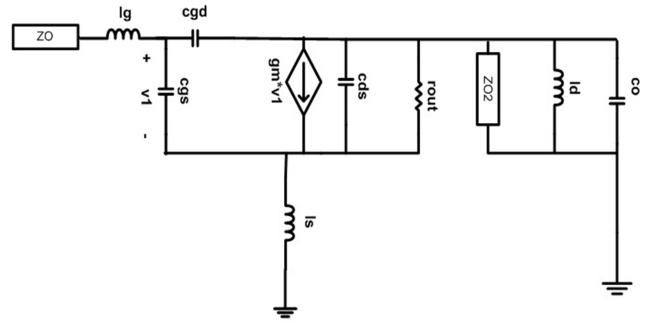
To clarify, each stage is designed separately in order to fulfil the purpose of the design. The first stage is designed to have an acceptable input matching. Plus, the elements and bias are adjusted to bring down the power dissipation. The input impedance of the stage is given by [11-13]:

$$z_{in} \approx s \times (lg + ls) + \frac{1}{s \times cgs} + \frac{gm \times ls}{cgs} \quad (1)$$

The approximation in (1) might bring around considerable errors in calculation, thus needing more precise calculation. To commence the design process precisely, each stage is clarified separately. The first stage, CS LNA, is depicted in figure 2 and its small signal equivalent circuit is demonstrated in figure 3.



**Figure 2.** Stage one (common-source).



**Figure 3.** Small signal equivalent circuit of stage one.

The small signal equivalent circuit is solved with the intention of extracting input impedance, output impedance, and gain. The input impedance is given:

$$Zin_{CS} = \frac{NUMZINFIRST}{DENZINFIRST}$$

$$\begin{aligned} NUMZINFIRST = & (rout \times zo2 + ld \times ls \times s^2 \\ & + ld \times rout \times s + ld \times s \times zo2 + ls \times s \times zo2 + \\ & gm \times ls \times rout \times s \times zo2 + cgs \times ld \times lg \times ls \times \\ & s^4 + cgd \times ld \times lg \times ls \times s^4 + cgs \times ld \times lg \times \\ & rout \times s^3 + cgd \times ld \times lg \times rout \times s^3 + cgs \times \\ & ld \times ls \times rout \times s^3 + cds \times ld \times ls \times rout \times s^3 \\ & + gm \times ld \times ls \times rout \times s^2 + cgs \times ld \times lg \times s^3 \\ & \times zo2 + cgd \times ld \times lg \times s^3 \times zo2 + cgs \times ld \times \\ & ls \times s^3 \times zo2 + cgd \times ld \times ls \times s^3 \times zo2 + cgs \\ & \times lg \times ls \times s^3 \times zo2 + cgd \times lg \times ls \times s^3 \times zo2 \\ & + co \times ld \times ls \times s^3 \times zo2 + cgd \times ld \times rout \times \\ & s^2 \times zo2 + cds \times ld \times rout \times s^2 \times zo2 + cgs \times \\ & lg \times rout \times s^2 \times zo2 + cgd \times lg \times rout \times s^2 \times \\ & zo2 + cgs \times ls \times rout \times s^2 \times zo2 + cds \times ls \times \\ & rout \times s^2 \times zo2 + co \times ld \times rout \times s^2 \times zo2 + \\ & cgs \times cgd \times ld \times lg \times ls \times rout \times s^5 + cgs \times cds \\ & \times ld \times lg \times ls \times rout \times s^5 + cgd \times cds \times ld \times lg \\ & \times ls \times rout \times s^5 + cgd \times gm \times ld \times lg \times ls \times rout \\ & \times s^4 + cgs \times co \times ld \times lg \times ls \times s^5 \times zo2 + cgd \times \\ & co \times ld \times lg \times ls \times s^5 \times zo2 + cgs \times cgd \times ld \times lg \\ & \times rout \times s^4 \times zo2 + cgs \times cds \times ld \times lg \times rout \times s^4 \\ & \times zo2 + cgd \times cds \times ld \times lg \times rout \times s^4 \times zo2 + \\ & cgs \times cgd \times ld \times ls \times rout \times s^4 \times zo2 + cgs \times cds \\ & \times ld \times ls \times rout \times s^4 \times zo2 + cgd \times cds \times ld \times \\ & ls \times rout \times s^4 \times zo2 + cgs \times cgd \times lg \times ls \times rout \times \\ & s^4 \times zo2 + cgs \times cds \times lg \times ls \times rout \times s^4 \times \\ & zo2 + cgs \times co \times ld \times lg \times rout \times s^4 \times zo2 + \end{aligned} \quad (2)$$

$$\begin{aligned}
& cgd \times co \times ld \times lg \times rout \times s^4 \times zo2 + cgs \times \\
& co \times ld \times ls \times rout \times s^4 \times zo2 + cds \times co \times ld \\
& \times ls \times rout \times s^4 \times zo2 + cgd \times gm \times ld \times lg \times \\
& rout \times s^3 \times zo2 + cgd \times gm \times ld \times ls \times rout \times \\
& s^3 \times zo2 + cgd \times gm \times lg \times ls \times rout \times s^3 \times zo2 \\
& + co \times gm \times ld \times ls \times rout \times s^3 \times zo2 + cgs \times \\
& cgd \times co \times ld \times lg \times ls \times rout \times s^6 \times zo2 + cgs \\
& \times cds \times co \times ld \times lg \times ls \times rout \times s^6 \times zo2 + cgd \\
& \times cds \times co \times ld \times lg \times ls \times rout \times s^6 \times zo2 + cgd \\
& \times co \times gm \times ld \times lg \times ls \times rout \times s^5 \times zo2) \\
\\
& DENZINFIRST = (s \times (cgs \times rout \times zo2 + \\
& cgd \times rout \times zo2 + cgs \times ld \times rout \times s + cgd \\
& \times ld \times rout \times s + cgs \times ld \times s \times zo2 + cgd \times ld \\
& \times s \times zo2 + cgs \times ls \times s \times zo2 + cgd \times ls \times s \times \\
& zo2 + cgs \times ld \times ls \times s^2 + cgd \times ld \times ls \times s^2 + \\
& cgs \times cgd \times ld \times ls \times rout \times s^3 + cgs \times cds \times ld \\
& \times ls \times rout \times s^3 + cgd \times cds \times ld \times ls \times rout \times s^3 \\
& + cgd \times gm \times ld \times ls \times rout \times s^2 + cgs \times co \times ld \\
& \times ls \times s^3 \times zo2 + cgd \times co \times ld \times ls \times s^3 \times zo2 + \\
& cgs \times cgd \times ld \times rout \times s^2 \times zo2 + cgs \times cds \times \\
& ld \times rout \times s^2 \times zo2 + cgd \times cds \times ld \times rout \times \\
& s^2 \times zo2 + cgs \times cgd \times ls \times rout \times s^2 \times zo2 + cgd \times cds \times \\
& ls \times rout \times s^2 \times zo2 + cgs \times co \times ld \times rout \times s^2 \\
& \times zo2 + cgd \times co \times ld \times rout \times s^2 \times zo2 + cgd \\
& \times gm \times ld \times rout \times s \times zo2 + cgd \times gm \times ls \times \\
& rout \times s \times zo2 + cgs \times cgd \times co \times ld \times ls \times rout \\
& \times s^4 \times zo2 + cgs \times cds \times co \times ld \times ls \times rout \times s^4 \\
& \times zo2 + cgd \times cds \times co \times ld \times ls \times rout \times s^4 \times \\
& zo2 + cgd \times co \times gm \times ld \times ls \times rout \times s^3 \times zo2)
\end{aligned}$$

In which:

rout: the output resistor of M1

zo2= the impedance of output port

cgd: the capacitor seen through gate-to-drain of M1

cds: the capacitor seen through drain-to-source of M1

cgs: the capacitor seen through gate-to-source of M1

gm: transconductance of M1

$$s : 2 \times \pi \times f \times \sqrt{-1}$$

f: frequency

In order to compare two formulas, the simulation results performed by HSPICE with TSMC 0.18  $\mu\text{m}$  RF are compared in figure 4.

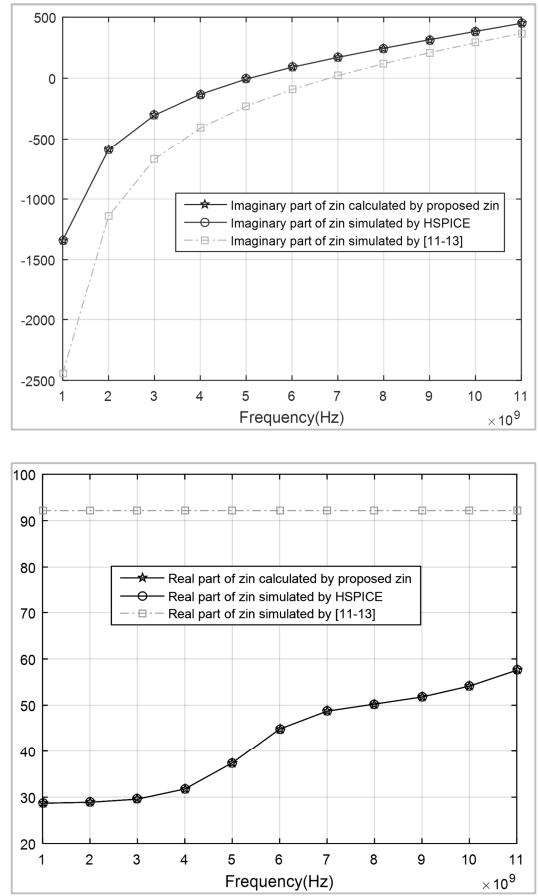


Figure 4. The comparison of imaginary and real part of proposed zin.

The following conclusions can be deduced from figure 4:

1. The error between the proposed zin and simulated results are approximately zero.
2. The error coming from (1) in imaginary part is noticeable but negligible.
3. The error coming from (1) in real part is considerable and not negligible.
4. It is implied by (1) that the elements in the output of M1 do not play any role in zin. In (2), however, it is proved that all elements in the output of the circuits affect zin directly.
5. It is implied by (1) that the real part of zin does not vary via frequency. In (2) demonstrates that it is clearly altered.

The results coming from (1) might be afflicted with the drastic error in real part. For instance, at 7 GHz the real part is 48 from simulation versus 92 from (1). The error is about 90%, which cannot lead into a precise design. These comments are applicable to output impedance and gain of the LNA. Indeed, S11, S22, and S21 are calculated by [14]:

$$\begin{aligned}
S11 &= \frac{zin - zo}{zin + zo} \\
S22 &= \frac{zout - zo}{zout + zo} \\
S21 &= (1 + s11) \times \left( \frac{vout}{vin} \right) \\
S12 &= (1 + s22) \times \left( \frac{vin}{vout} \right)
\end{aligned} \tag{3}$$

Owing to the fact that all the s-parameters are dependent upon input and output impedance, the error in both of them deteriorates the whole design. In addition, the output impedance of the first stage is given by:

$$\begin{aligned}
 & ls \times rout \times s^3 \times zo + cgs \times co \times ld \times rout \times s^3 \times \\
 & zo + cgd \times co \times ld \times rout \times s^3 \times zo + cgd \times gm \\
 & \times ld \times rout \times s^2 \times zo + cgd \times gm \times ls \times rout \times s^2 \\
 & \times zo + cgs \times cgd \times co \times ld \times lg \times ls \times rout \times s^6 \\
 & + cgs \times cds \times co \times ld \times lg \times ls \times rout \times s^6 + cgd \\
 & \times cds \times co \times ld \times lg \times ls \times rout \times s^6 + cgd \times co \\
 & \times gm \times ld \times lg \times ls \times rout \times s^5 + cgs \times cgd \times co \\
 & \times ld \times ls \times rout \times s^5 \times zo + cgs \times cds \times co \times ld \times \\
 & ls \times rout \times s^5 \times zo + cgd \times cds \times co \times ld \times ls \times \\
 & rout \times s^5 \times zo + cgd \times co \times gm \times ld \times ls \times rout \\
 & \times s^4 \times zo
 \end{aligned}$$

The gain is given by:

$$gain_{CS} = \frac{NUMGAINFIRST}{DENGAINFIRST}$$

$$NUMGAINFIRST = (ld \times s \times zo2 \times (cgs \times ls \\ \times s^2 - gm \times rout + cgd \times ls \times s^2 + cgd \times rout \\ \times s + cgs \times cgd \times ls \times rout \times s^3 + cgs \times cds \times \\ ls \times rout \times s^3 + cgd \times cds \times ls \times rout \times s^3 + \\ cgd \times gm \times ls \times rout \times s^2)) \quad (5)$$

$$\begin{aligned}
DENGAINFIRST = & (rout \times zo2 + ld \times ls \times s^2 \\
& + ld \times rout \times s + ld \times s \times zo2 + ls \times s \times zo2 + \\
& gm \times ls \times rout \times s \times zo2 + cgs \times rout \times s \times zo \\
& \times zo2 + cgd \times rout \times s \times zo \times zo2 + cgs \times ld \times \\
& lg \times ls \times s^4 + cgd \times ld \times lg \times ls \times s^4 + cgs \times \\
& ld \times lg \times rout \times s^3 + cgd \times ld \times lg \times rout \times \\
& s^3 + cgs \times ld \times ls \times rout \times s^3 + cds \times ld \times ls \\
& \times rout \times s^3 + gm \times ld \times ls \times rout \times s^2 + cgs \\
& \times ld \times lg \times s^3 \times zo2 + cgd \times ld \times lg \times s^3 \times \\
& zo2 + cgs \times ld \times ls \times s^3 \times zo + cgd \times ld \times ls \\
& \times s^3 \times zo + cgs \times ld \times ls \times s^3 \times zo2 + cgd \times \\
& ld \times ls \times s^3 \times zo2 + cgs \times lg \times ls \times s^3 \times zo2 \\
& + cgd \times lg \times ls \times s^3 \times zo2 + co \times ld \times ls \times s^3
\end{aligned}$$

$$\begin{aligned}
& \times zo2 + cgs \times ld \times rout \times s^2 \times zo + cgd \times ld \times rout \\
& \times s^2 \times zo + cgd \times ld \times rout \times s^2 \times zo2 + cds \times ld \times \\
& rout \times s^2 \times zo2 + cgs \times lg \times rout \times s^2 \times zo2 + cgd \\
& \times lg \times rout \times s^2 \times zo2 + cgs \times ls \times rout \times s^2 \times zo2 \\
& + cds \times ls \times rout \times s^2 \times zo2 + co \times ld \times rout \times s^2 \times \\
& zo2 + cgs \times ld \times s^2 \times zo \times zo2 + cgd \times ld \times s^2 \times zo \\
& \times zo2 + cgs \times ls \times s^2 \times zo \times zo2 + cgd \times ls \times s^2 \times zo \\
& \times zo2 + cgs \times cgd \times ld \times lg \times ls \times rout \times s^5 + cgs \times \\
& cds \times ld \times lg \times ls \times rout \times s^5 + cgd \times cds \times ld \times lg \times \\
& ls \times rout \times s^5 + cgd \times gm \times ld \times lg \times ls \times rout \times s^4 + \\
& cgs \times co \times ld \times lg \times ls \times s^5 \times zo2 + cgd \times co \times ld \times lg \\
& \times ls \times s^5 \times zo2 + cgs \times cgd \times ld \times lg \times rout \times s^4 \times zo2 \\
& + cgs \times cds \times ld \times lg \times rout \times s^4 \times zo2 + cgd \times cds \times \\
& ld \times lg \times rout \times s^4 \times zo2 + cgs \times cgd \times ld \times ls \times rout \\
& \times s^4 \times zo + cgs \times cds \times ld \times ls \times rout \times s^4 \times zo + cgs \\
& \times cgd \times ld \times ls \times rout \times s^4 \times zo2 + cgd \times cds \times ld \times ls \\
& \times rout \times s^4 \times zo + cgs \times cds \times ld \times ls \times rout \times s^4 \times \\
& zo2 + cgd \times cds \times ld \times ls \times rout \times s^4 \times zo2 + cgs \times \\
& cgd \times lg \times ls \times rout \times s^4 \times zo2 + cgs \times cds \times lg \times ls \times \\
& rout \times s^4 \times zo2 + cgd \times cds \times lg \times ls \times rout \times s^4 \times zo2 \\
& + cgs \times co \times ld \times lg \times rout \times s^4 \times zo2 + cgd \times co \times ld \times \\
& lg \times rout \times s^4 \times zo2 + cgs \times co \times ld \times ls \times rout \times s^4 \times \\
& zo2 + cds \times co \times ld \times ls \times rout \times s^4 \times zo2 + cgd \times gm \times \\
& ld \times lg \times rout \times s^3 \times zo2 + cgd \times gm \times ld \times ls \times rout \times \\
& s^3 \times zo + cgd \times gm \times ld \times ls \times rout \times s^3 \times zo2 + cgd \times \\
& gm \times lg \times ls \times rout \times s^3 \times zo2 + co \times gm \times ld \times ls \times \\
& rout \times s^3 \times zo2 + cgs \times co \times ld \times ls \times s^4 \times zo \times zo2 + \\
& cgd \times co \times ld \times ls \times s^4 \times zo \times zo2 + cgs \times cgd \times ld \times \\
& rout \times s^3 \times zo \times zo2 + cgs \times cds \times ld \times rout \times s^3 \times \\
& zo \times zo2 + cgd \times cds \times ld \times rout \times s^3 \times zo \times zo2 +
\end{aligned}$$

$$\begin{aligned}
& cgs \times cgd \times ls \times rout \times s^3 \times zo \times zo2 + cgs \times cds \\
& \times ls \times rout \times s^3 \times zo \times zo2 + cgd \times cds \times ls \times rout \\
& \times s^3 \times zo \times zo2 + cgs \times co \times ld \times rout \times s^3 \times zo \times \\
& zo2 + cgd \times co \times ld \times rout \times s^3 \times zo \times zo2 + cgd \\
& \times gm \times ld \times rout \times s^2 \times zo \times zo2 + cgd \times gm \times ls \times \\
& rout \times s^2 \times zo \times zo2 + cgs \times cgd \times co \times ld \times lg \times \\
& ls \times rout \times s^6 \times zo2 + cgs \times cds \times co \times ld \times lg \times ls \\
& \times rout \times s^6 \times zo2 + cgd \times cds \times co \times gm \times ld \times lg \times ls \\
& \times rout \times s^5 \times zo2 + cgs \times cgd \times co \times ld \times ls \times rout \\
& \times s^5 \times zo \times zo2 + cgs \times cds \times co \times ld \times ls \times rout \\
& \times s^5 \times zo \times zo2 + cgd \times cds \times co \times gm \times ld \times ls \times rout \\
& \times s^5 \times zo \times zo2 + cgd \times co \times gm \times ld \times ls \times rout \\
& \times s^4 \times zo \times zo2)
\end{aligned}$$

### 3. Cascode LNA

The second stage of the LNA is a cascode LNA. Indeed, the main purpose of utilizing cascode is that the gain of the final LNA is increased and the S12 decline significantly. The cascode LNA and its equivalent circuit are demonstrated in figure 5 and figure 6.

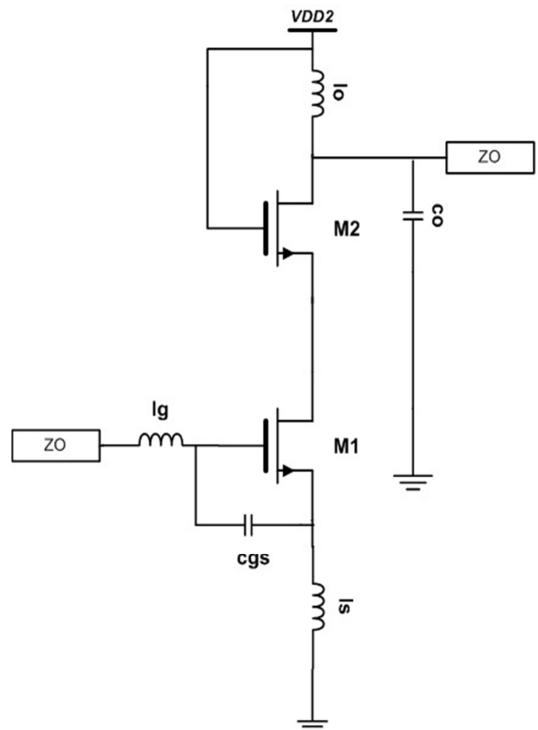


Figure 5. Cascode LNA.

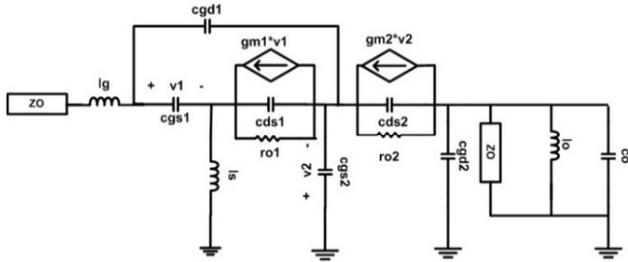


Figure 6. Small signal equivalent circuit of cascode LNA.

The gain of cascode is given by:

$$gainscas = \frac{numcas}{denas} \quad (6)$$

The details of (6) is represented in the Appendix. The formulas might be considered as long and complicated. Nevertheless, they are supposed to be solved by MATLAB and precision should not be sacrificed for simplicity or approximation.

#### 4. Biasing and Design

Biasing is a significant factor by which power consumption can be manipulated. As it can be seen in figure 1, two divergent voltage supplies are used to bias the circuit. This technique might bring down the power consumption of

the circuit considerably. The main purpose of the CS LNA at the first stage is a proper input impedance matching. On the other hand, the Cascode LNA is used to increase the gain. The first goal can be achieved by  $VDD1=0.5$  volt. Therefore, it is not necessary to waste power in the first stage. The second stage, however, might need a bigger voltage to have a better gain and this can be obtained by  $VDD2=0.7$  volt.

Another aspect of designing the LNA is the width of transistors, defining the current of the transistors. Plus, all transistors should be adjusted appropriately in the strong, moderate, or weak inversion to reduce the power dissipation. In this paper, the width of all transistors is set to 80  $\mu\text{m}$ . M1 and M2 are biased to operate in the strong inversion region versus M3 operating in the moderate inversion region.

#### 5. Results

The proposed LNA is simulated at 5 GHz by Advanced Design System (ADS) and 0.18  $\mu\text{m}$  CMOS Process is used for all transistors. The performance is evaluated in different situations, compared in table 1. First, the LNA is analysed by lumped elements except transistors. Second, all elements, including inductors, capacitors, and resistors are substituted with their counterpart elements in 0.18  $\mu\text{m}$  technology. Ultimately, both circumstances are scrutinized by increasing source voltages and the trade-offs are mentioned.

Table 1. Comparison of the performance against voltage sources and elements.

Performance	VDD1=0.5 LUMPED	VDD1=0.7 LUMPED	VDD1=0.9 LUMPED	VDD1=0.5 REAL	VDD1=0.7 REAL	VDD1=0.9 REAL
NF (dB)	0.49	0.45	0.368	1.247	1.164	1.044
S11 (dB)	-17	-15	-15	-14	-14	-16
S12 (dB)	-34	-34	-34	-36	-36	-36
S21 (dB)	21.9	22	24	15	15	17
*Pdiss ( $\mu\text{W}$ )	248+288=536	379+287=666	527+423=950	246+286=532	377+286=663	524+420=944

\*The first figure is the Pdiss for the first stage, and the second is for the second stage

The results are illustrated from figure 7 to figure 22. As it is expected, the results coming from lumped-elements are more appropriate than the results with real elements.

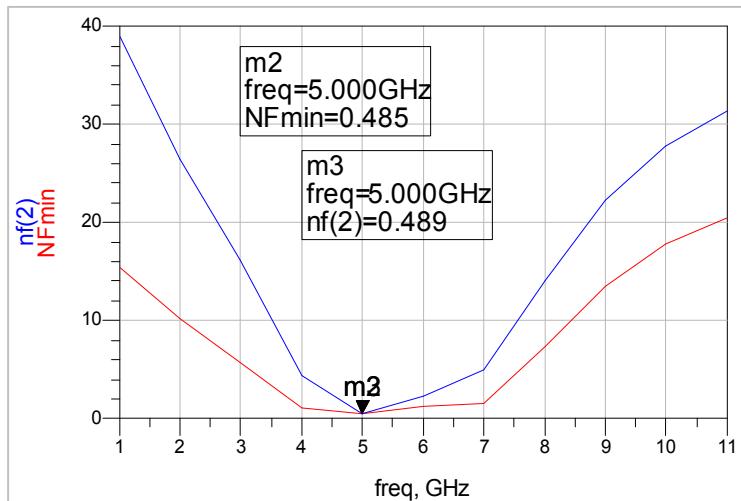


Figure 7. Noise Figure with lumped-elements.

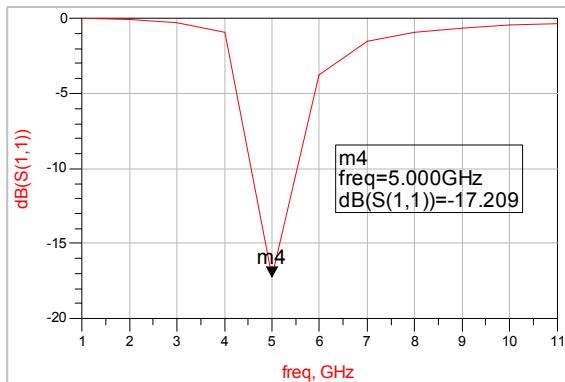
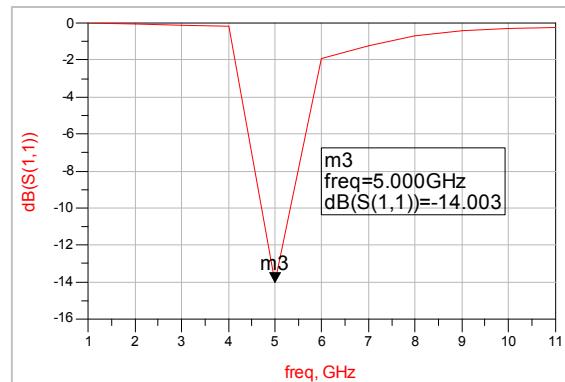
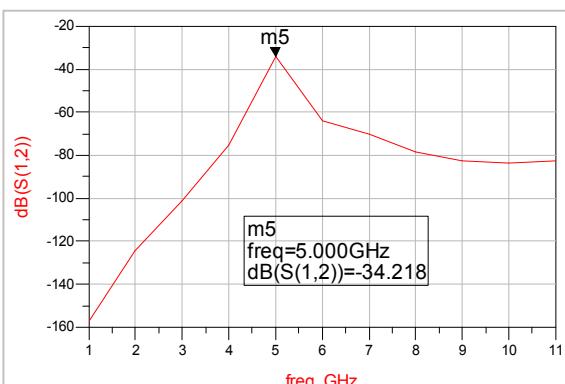
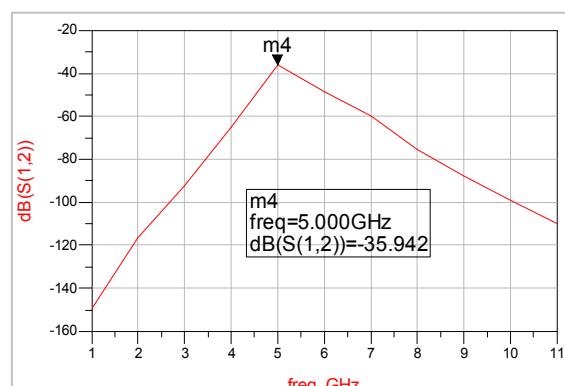
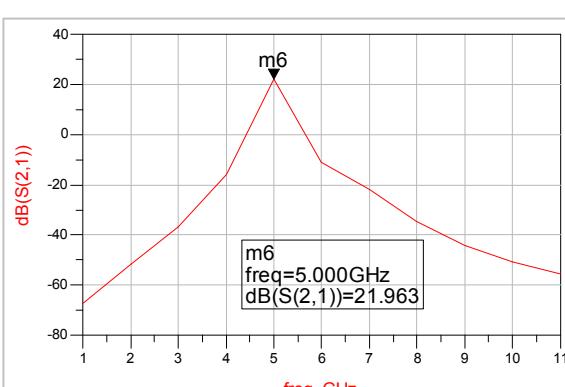
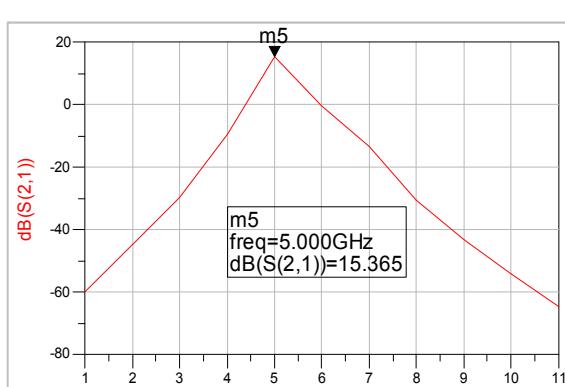
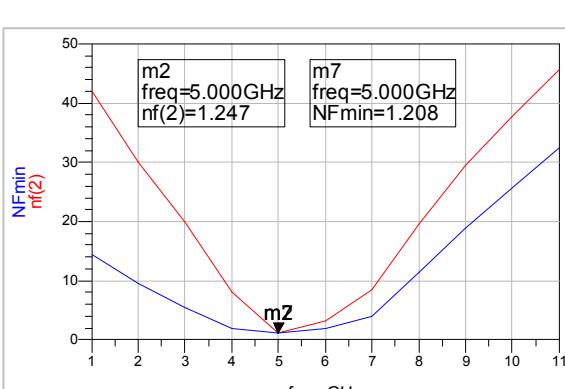
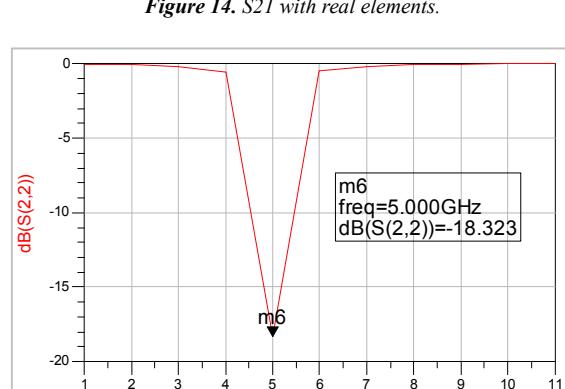
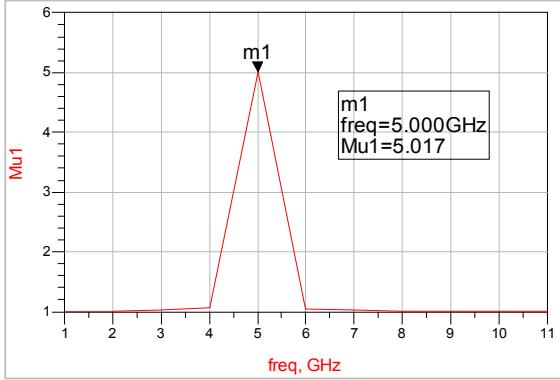
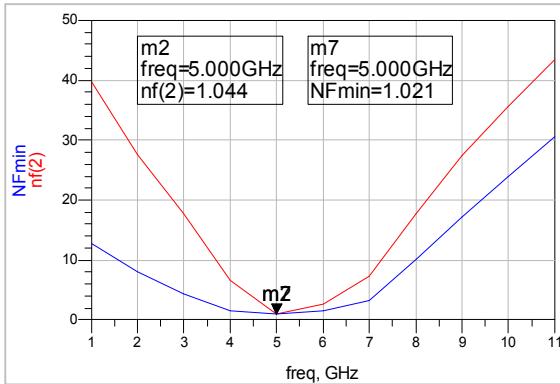
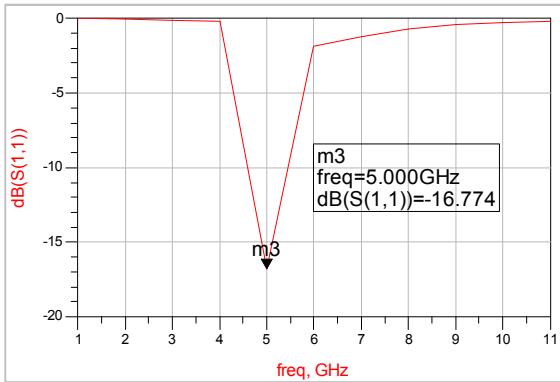
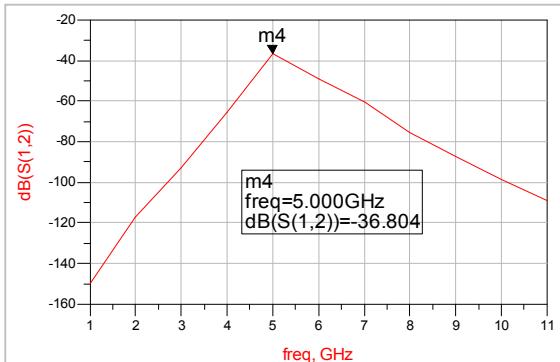
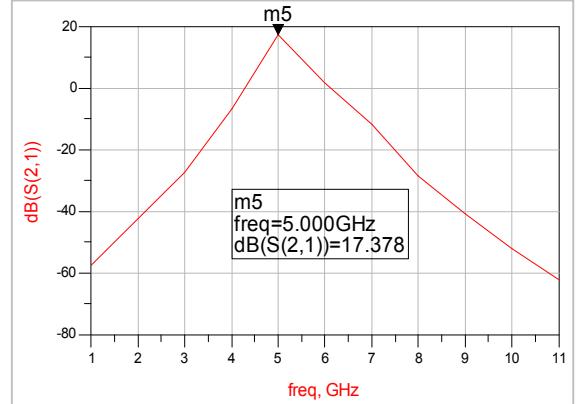
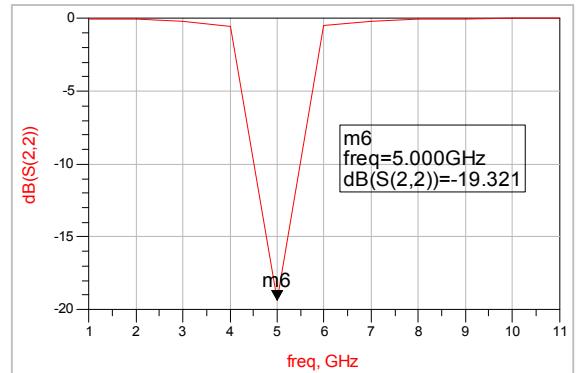
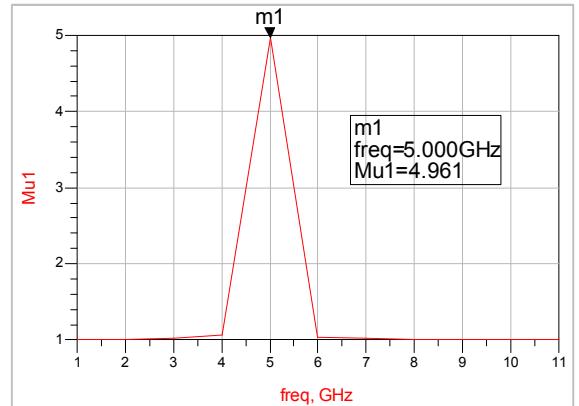
Figure 8.  $S_{11}$  with Lumped-elements.Figure 12.  $S_{11}$  with real elements.Figure 9.  $S_{12}$  with Lumped-elements.Figure 13.  $S_{12}$  with real elements.Figure 10.  $S_{21}$  with Lumped-elements.Figure 14.  $S_{21}$  with real elements.

Figure 11. Noise Figure with real elements.

Figure 15.  $S_{22}$  with real elements.

Figure 16.  $\mu$  Stability with real elements.Figure 17. Noise Figure with real components and  $VDD1=VDD2=0.9$ .Figure 18.  $S11$  with real components and  $VDD1=VDD2=0.9$ .Figure 19.  $S12$  with real components and  $VDD1=VDD2=0.9$ .Figure 20.  $S21$  with real components and  $VDD1=VDD2=0.9$ .Figure 21.  $S22$  with real components and  $VDD1=VDD2=0.9$ .Figure 22.  $\mu$  Stability with real components and  $VDD1=VDD2=0.9$ .

In addition, the performance of an LNA has been evaluated by S-parameters, power dissipation, gain, and Noise figure. The aforementioned items can be compared separately or be used together to form a criterion by which the performance might be scrutinized better. To fulfil the purpose, three divergent figures of merit (FOM) have been proposed [13], [15-16].

$$FOM1 = \frac{20 \times \log |S21|}{P_{dc}} \quad (7)$$

$$FOM2 = \frac{|S21|}{|NF - 1| \times P_{dc}} \quad (8)$$

$$FOM3 = \frac{Gain[abs] \times IIP3[mW] \times f_c[GHz]}{|NF - 1| [abs] \times P_{dc}[mW]} \quad (9)$$

Owing to the fact that all significant parameters participate in the figure of merit, the performance of the LNA might be evaluated more precisely. The performance of the LNA is compared with other state-of-the-art in table 2.

The stability of an LNA can be guaranteed by mu ( $\mu$ ) stability test given by:

$$\mu = \frac{1 - |S11|^2 - |S22|^2 + |\Delta|^2}{2 \times |S12|^2 \times |S21|^2} \quad (10)$$

$$\Delta = S11 \times S22 - S12 \times S21$$

The LNA is unconditionally stable provided that  $\mu$  is larger than one. Plus, the larger  $\mu$  is, the more stable the LNA will be.

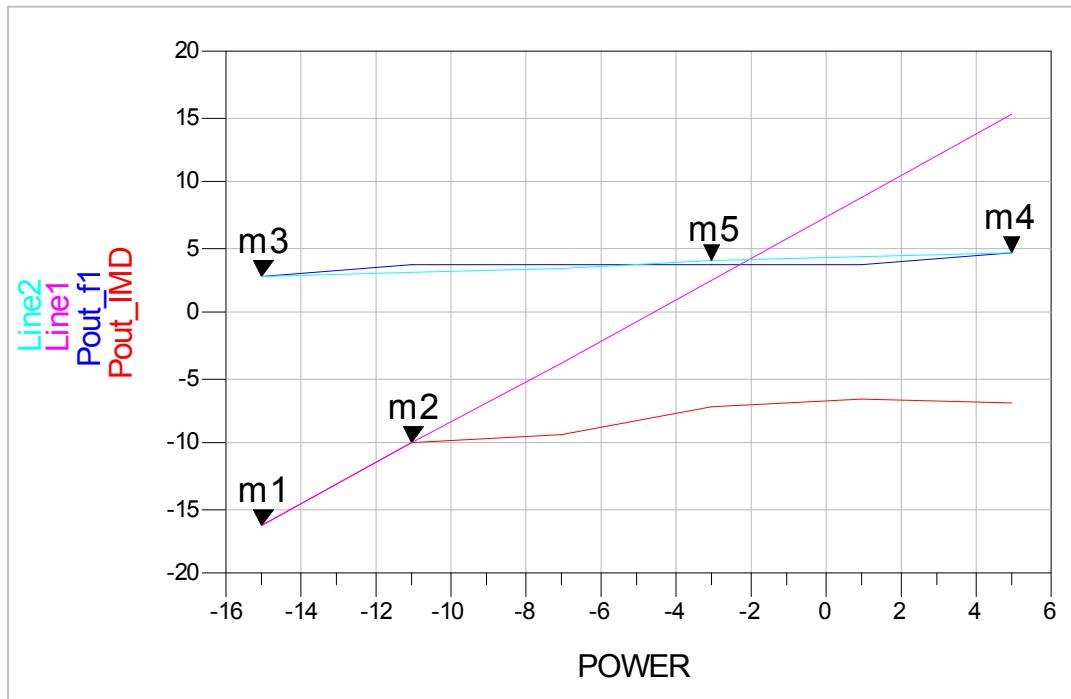


Figure 23. IIP3 with real component and VDD1=0.5 and VDD2=0.7.

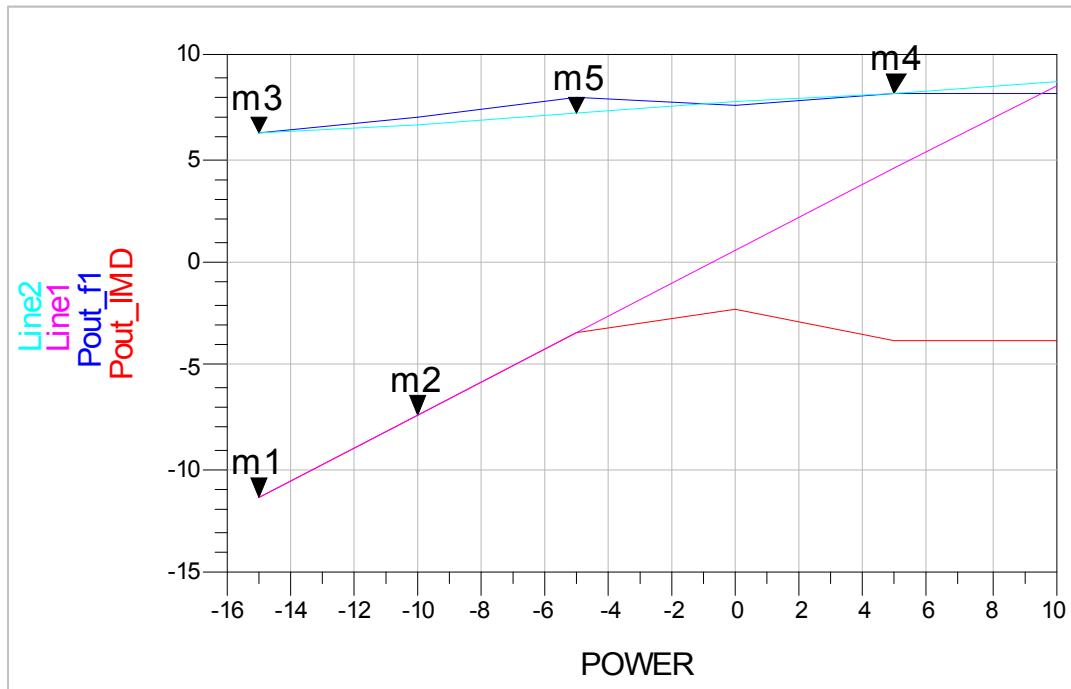


Figure 24. IIP3 with real component and VDD1=0.9 and VDD2=0.9.

The linearity of the LNA, which is demonstrated in figure 23 and figure 24, is enhanced by increasing voltage supply to 0.9 volt. It is another trade-off between power consumption and linearity.

**Table 2. PERFORMANCE SUMMARY AND COMPARISON WITH OTHER STATE-OF-THE-ART.**

TECHNOLOGY	Frequency	Supply voltage	Power (diss)	S21	NF	S11	S22	IIP3	FOM1	FOM2	FOM3	
unit	$\mu\text{m}$	GHz	V	mW	dB	dB	dB	dBm	dB/mW	1/mW	-	
This work	0.18	5	Vdd1=0.5, Vdd2=0.7	0.532	15	1.25	-14	-18	-3	28	84	211
This work	0.18	5	Vdd1=vdd2=0.9	0.944	17	1.05	-16	-19	9	18	300	1.1914e+04
[17]	0.09	5.5	1.2	9.72	13	2.7	-11.7	-14	-3.25	1.34	0.53	1.39
[18]	0.09	5.5	0.6	2.1	11.2	3.6	-28	-14	-8.6	5.33	1.34	1.02
[19]	0.18	5	1.5	15	20	3.5	-20	-20	-9	1.33	0.54	0.34
[20]	0.18	5.8	1	22.2	13.2	2.5	-5.3	-10.3	-	0.59	0.26	-
	0.18	5.8	0.7	12.5	7	2.68	-7.1	-12.3	-	0.56	0.21	-
[21]	0.25	5.2	2	10	10	3	-30	-	0.3	1	0.32	1.77
	0.25	5.2	2	10	11	2.17	-45	-	0.3	1.1	0.55	3.05
[22]	0.25	5.25	3	12	14.4	2.8	-11.5	-12.3	-1.5	1.2	0.48	1.8
	0.25	5.25	3	24	16	2.5	-12.3	-11.9	-1.5	0.67	0.34	1.26
[23]	0.25	5.8	2	10	8	4.8	-23.5	-10.3	10	0.8	0.12	6.84
[24]	0.18	5.7	1.8	3.96	11.47	3.4	-14	-17	-	2.89	0.79	-
[25]	0.18	5.7	1	3.2	16.4	3.5	-11	-15	-	5.12	1.67	-
[26]	0.13	5.1	0.4	1.03	10.3	5.3	-17.7	-11.4	-	10.02	1.33	-
[27]	0.09	5.5	1.2	9.72	12.3	2.7	-10.3	-19	-3	1.27	0.49	0.68
[28]	0.09	5.5	0.6	1	9.2	3.6	-10	-14	-7.25	9.01	2.23	2.3
	0.09	5.5	0.8	5.4	14.4	2.9	-13.4	-10.7	-6.2	2.67	1.02	1.35
[29]	0.18	5	0.6	0.9	9.2	4.5	-12	-21	-16	10.22	1.76	0.23
[30]	0.18	5.2	0.6	1.08	10	3.37	-13.4	-10.6	-8.6	9.26	2.5	1.78
	0.18	5	0.6	1.68	14.1	3.65	-12.7	-14	-17.1	8.39	2.29	0.23
[31]	0.18	5.2	1.8	12.4	16.5	1.1	<-20	-13	-11.5	1.33	1.87	7.61
[32]	0.18	5.8	1.8	3.42	9.4	2.5	-13.3	-14.8	-7.6	2.75	1.11	1.16
[33]	0.18	5.4	1.8	2.7	21	2.8	<-10	-	-23	7.78	4.59	0.125
[34]	0.09	2.6-10.2	1.2	7.2	12.5	3-7	<-9	-	-	1.74	0.47	-
[35]	0.13	5.65	1.2	6.4	14.9	4.8	-324	-	-4.2	2.33	0.43	0.99
[36]	0.18	5	1.5	12	11	0.95	-33	-13	5	0.92	1.21	187
[13]	0.18	5.8	0.6	0.798	11.21	3.22	-19.19	-14.67	-9	14.04	4.14	3
	0.18	5.8	0.6	0.834	13.92	3.32	-12.74	-13.38	-11.5	16.69	5.19	2.1

## 6. Conclusion

In this paper an LNA is designed with the intention of low power consumption, thus prolonging the life of the device. In fact, the design revolves around precise computation for input impedance, output impedance, and gain. Indeed, owing to the fact that all elements, which include capacitors and inductors, should be calculated via input impedance and output impedance, the error stemming from the approximation in their formulas impacts the design extremely. An approach is proposed to use two different supply voltages to decrease the first stage power consumption. Indeed, the decline in the voltage supply of the first stage is a contributing factor for an appropriate power

consumption. In addition, trade-off between power consumption and gain, NF, and IIP3 can be observed. Indeed, the power consumption is increased from 532  $\mu\text{W}$  to 944  $\mu\text{W}$  by boosting VDD1, and VDD2 to 0.9 volts. Plus, NF, S11, IIP3, and S21 are enhanced from 1.247, -14, -3, and 15 to 1.044, -16, 9, and 17 respectively. Although the technology has been scaled down to nanometre, the topology and calculation proposed are applicable to other technologies, i.e. 0.13 $\mu\text{m}$ , 0.09 $\mu\text{m}$ , and so on. Despite the fact that the LNA is not implemented, it is declared by all other state-of-the-art that the implemented circuit's results are close to the simulated circuit. Hence, it is deducible that if the LNA be implemented, the results might be close to the simulated results.

## Appendix

### CASCODE GAIN

$$gain_{cas} = \frac{num_{cas}}{den_{cas}} \quad (11)$$

$$\begin{aligned}
num_{cas} = & (lo \times s \times zo \times (gm2 \times ro2 + cds2 \times ro2 \times s + 1) \times (cgs1 \times ls \times s^2 - gm1 \times ro1 + cgd1 \times ls \times s^2 + cgd1 \times ro1 \times s + cgs1 \times cgd1 \\
& \times ls \times ro1 \times s^3 + cgs1 \times cds1 \times ls \times ro1 \times s^3 + cgd1 \times cds1 \times ls \times ro1 \times s^3 + cgd1 \times gm1 \times ls \times ro1 \times s^2)) \\
den_{cas} = & ro1 \times zo + ro2 \times zo + ls \times lo \times s + lo \times ro1 \times s + lo \times ro2 \times s + ls \times s \times zo + lo \times s \times zo + gm2 \times ro1 \times ro2 \times zo + cgs1 \\
& \times ro1 \times s \times zo^2 + cgs1 \times ro2 \times s \times zo^2 + cgd1 \times ro1 \times s \times zo^2 + cgd1 \times ro2 \times s \times zo^2 + cgs1 \times ls \times s^2 \times zo^2 + cgd1 \times ls \times s^2 \times \\
& zo^2 + cgs1 \times lo \times s^2 \times zo^2 + cgd1 \times lo \times s^2 \times zo^2 + gm2 \times lo \times ro1 \times ro2 \times s + gm1 \times ls \times ro1 \times s \times zo + gm2 \times ls \times ro2 \times s \times \\
& zo + cgs2 \times ro1 \times ro2 \times s \times zo + cgd1 \times ro1 \times ro2 \times s \times zo + cds1 \times ro1 \times ro2 \times s \times zo + cds2 \times ro1 \times ro2 \times s \times zo + cgs1 \times ls \times \\
& lg \times lo \times s^4 + cgd1 \times ls \times lg \times lo \times s^4 + cgs1 \times ls \times lo \times ro1 \times s^3 + cgs1 \times ls \times lo \times ro2 \times s^3 + cgs2 \times ls \times lo \times ro2 \times s^3 + \\
& cgd1 \times ls \times lo \times ro2 \times s^3 + cds1 \times ls \times lo \times ro1 \times s^3 + cds2 \times ls \times lo \times ro2 \times s^3 + cgs1 \times lg \times lo \times ro1 \times s^3 + cgs1 \times lg \times lo \times \\
& ro2 \times s^3 + cgd1 \times lg \times lo \times ro1 \times s^3 + cgd1 \times lg \times lo \times ro2 \times s^3 + gm1 \times ls \times lo \times ro1 \times s^2 + gm2 \times ls \times lo \times ro2 \times s^2 + cgs2 \times \\
& lo \times ro1 \times ro2 \times s^2 + cgd1 \times lo \times ro1 \times ro2 \times s^2 + cds1 \times lo \times ro1 \times ro2 \times s^2 + cds2 \times lo \times ro1 \times ro2 \times s^2 + cgs1 \times ls \times lg \times s^3 \\
& \times zo + cgd1 \times ls \times lg \times s^3 \times zo + 2.0 \times cgs1 \times ls \times lo \times s^3 \times zo + cgs2 \times ls \times lo \times s^3 \times zo + 2.0 \times cgd1 \times ls \times lo \times s^3 \times zo + cgd2 \\
& \times ls \times lo \times s^3 \times zo + cgs1 \times lg \times lo \times s^3 \times zo + cgd1 \times lg \times lo \times s^3 \times zo + co \times ls \times lo \times s^3 \times zo + cgs1 \times ls \times ro1 \times s^2 \times zo + \\
& cgs1 \times ls \times ro2 \times s^2 \times zo + cgs2 \times ls \times ro2 \times s^2 \times zo + cgd1 \times ls \times ro2 \times s^2 \times zo + cds1 \times ls \times ro1 \times s^2 \times zo + cds2 \times ls \times ro2 \times \\
& s^2 \times zo + cgs1 \times lg \times ro1 \times s^2 \times zo + cgs1 \times lg \times ro2 \times s^2 \times zo + cgd1 \times lg \times ro1 \times s^2 \times zo + cgd1 \times lg \times ro2 \times s^2 \times zo + cgs1 \\
& \times lo \times ro1 \times s^2 \times zo + cgs1 \times lo \times ro2 \times s^2 \times zo + cgs2 \times lo \times ro1 \times s^2 \times zo + 2 \times cgd1 \times lo \times ro1 \times s^2 \times zo + cgd1 \times lo \times ro2 \times \\
& s^2 \times zo + cgd2 \times lo \times ro1 \times s^2 \times zo + cgd2 \times lo \times ro2 \times s^2 \times zo + cds1 \times lo \times ro1 \times s^2 \times zo + cds2 \times lo \times ro2 \times s^2 \times zo + co \times \\
& lo \times ro1 \times s^2 \times zo + co \times lo \times ro2 \times s^2 \times zo + cgs1 \times gm2 \times ro1 \times ro2 \times s \times zo^2 + cgd1 \times gm1 \times ro1 \times ro2 \times s \times zo^2 + cgd1 \times \\
& gm2 \times ro1 \times ro2 \times s \times zo^2 + cgs1 \times cgs2 \times ls \times lo \times s^4 \times zo^2 + cgs1 \times cgd2 \times ls \times lo \times s^4 \times zo^2 + cgs2 \times cgd1 \times ls \times lo \times s^4 \times \\
& zo^2 + cgd1 \times cgd2 \times ls \times lo \times s^4 \times zo^2 + cgs1 \times co \times ls \times lo \times s^4 \times zo^2 + cgd1 \times co \times ls \times lo \times s^4 \times zo^2 + cgs1 \times cgs2 \times ls \times \\
& ro2 \times s^3 \times zo^2 + cgs1 \times cgd1 \times ls \times ro1 \times s^3 \times zo^2 + cgs2 \times cgd1 \times ls \times ro2 \times s^3 \times zo^2 + cgs1 \times cds1 \times ls \times ro1 \times s^3 \times zo^2 + \\
& cgs1 \times cds2 \times ls \times ro2 \times s^3 \times zo^2 + cgd1 \times cds1 \times ls \times ro1 \times s^3 \times zo^2 + cgd1 \times cds2 \times ls \times ro2 \times s^3 \times zo^2 + cgs1 \times cgs2 \times lo \times \\
& ro1 \times s^3 \times zo^2 + cgs1 \times cgd1 \times lo \times ro1 \times s^3 \times zo^2 + cgs1 \times cgd2 \times lo \times ro1 \times s^3 \times zo^2 + cgs2 \times cgd1 \times lo \times ro1 \times s^3 \times zo^2 + \\
& cgs1 \times cgd1 \times lo \times ro1 \times s^3 \times zo^2 + cgs1 \times cgs1 \times lo \times ro1 \times s^3 \times zo^2 + cgd1 \times cgd2 \times lo \times ro1 \times s^3 \times zo^2 + cgs1 \times cgs2 \times lo \times \\
& ro2 \times s^3 \times zo^2 + cgd1 \times cgd2 \times lo \times ro2 \times s^3 \times zo^2 + cgd1 \times cds1 \times lo \times ro1 \times s^3 \times zo^2 + cgd1 \times cds2 \times lo \times ro2 \times s^3 \times zo^2 \\
& + cgs1 \times co \times lo \times ro1 \times s^3 \times zo^2 + cgs1 \times co \times lo \times ro2 \times s^3 \times zo^2 + cgd1 \times co \times lo \times ro1 \times s^3 \times zo^2 + cgd1 \times co \times lo \times ro2 \times \\
& s^3 \times zo^2 + cgs1 \times gm2 \times ls \times ro2 \times s^2 \times zo^2 + cgd1 \times gm1 \times ls \times ro1 \times s^2 \times zo^2 + cgd1 \times gm2 \times ls \times ro2 \times s^2 \times zo^2 + cgd1 \times \\
& gm1 \times lo \times ro1 \times s^2 \times zo^2 + cgs1 \times cgs2 \times ro1 \times ro2 \times s^2 \times zo^2 + cgs1 \times cgd1 \times ro1 \times ro2 \times s^2 \times zo^2 + cgs2 \times cgd1 \times ro1 \times ro2 \\
& \times s^2 \times zo^2 + cgs1 \times cds1 \times ro1 \times ro2 \times s^2 \times zo^2 + cgs1 \times cds2 \times ro1 \times ro2 \times s^2 \times zo^2 + cgd1 \times cds1 \times ro1 \times ro2 \times s^2 \times zo^2 + \\
& cgd1 \times cds2 \times ro1 \times ro2 \times s^2 \times zo^2 + gm1 \times gm2 \times ls \times ro1 \times ro2 \times s \times zo + cgs1 \times cgs2 \times ls \times lg \times lo \times ro2 \times s^5 + cgs1 \times cgd1
\end{aligned}$$









$$\begin{aligned}
& \times lo \times ro1 \times ro2 \times s^7 \times zo + cgs1 \times cds1 \times cds2 \times co \times ls \times lg \times lo \times ro1 \times ro2 \times s^7 \times zo + cgd1 \times cds1 \times cds2 \times co \times ls \times lg \times lo \times \\
& ro1 \times ro2 \times s^7 \times zo + cgs1 \times cgd1 \times cgd2 \times gm2 \times ls \times lg \times lo \times ro1 \times ro2 \times s^6 \times zo + cgs2 \times cgd1 \times cgd2 \times gm1 \times ls \times lg \times lo \times \\
& ro1 \times ro2 \times s^6 \times zo + cgs1 \times cgd2 \times cds1 \times gm2 \times ls \times lg \times lo \times ro1 \times ro2 \times s^6 \times zo + cgs2 \times cgd1 \times cds2 \times gm1 \times ls \times lg \times lo \times \\
& ro1 \times ro2 \times s^6 \times zo + cgd1 \times cgd2 \times cds1 \times gm2 \times ls \times lg \times lo \times ro1 \times ro2 \times s^6 \times zo + cgd1 \times cgd2 \times cds2 \times gm1 \times ls \times lg \times lo \times \\
& ro1 \times ro2 \times s^6 \times zo + cgs1 \times cgd1 \times co \times gm2 \times ls \times lg \times lo \times ro1 \times ro2 \times s^6 \times zo + cgs2 \times cgd1 \times co \times gm1 \times ls \times lg \times lo \times ro1 \times \\
& ro2 \times s^6 \times zo + cgs1 \times co \times gm2 \times ls \times lg \times lo \times ro1 \times ro2 \times s^6 \times zo + cgd1 \times cds1 \times co \times gm2 \times ls \times lg \times lo \times ro1 \times ro2 \times \\
& s^6 \times zo + cgd1 \times cds2 \times co \times gm1 \times ls \times lg \times lo \times ro1 \times ro2 \times s^6 \times zo + cgd1 \times cgd2 \times gm1 \times gm2 \times ls \times lg \times lo \times ro1 \times ro2 \times s^5 \\
& \times zo + cgd1 \times co \times gm1 \times gm2 \times ls \times lg \times lo \times ro1 \times ro2 \times s^5 \times zo
\end{aligned}$$

In which:

$ro1$ : the output resistor of M1

$ro2$ : the output resistor of M2

$zo$ : the impedance of input or output port

$cgd1$ : the capacitor seen through gate-to-drain of M1

$cds1$ : the capacitor seen through drain-to-source of M1

$cgs1$ : the capacitor seen through gate-to-source of M1

$cgd2$ : the capacitor seen through gate-to-drain of M2

$cds2$ : the capacitor seen through drain-to-source of M2

$cgs2$ : the capacitor seen through gate-to-source of M2

$gm1$ : transconductance of M1

$gm2$ : transconductance of M2

$s : 2 \times \pi \times f \times \sqrt{-1}$

f: frequency

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