

Research Article

Formation and Facet Less Immersion of Discrete Al-Si Areas on Unpolished Wafers in Silicon Thermomigration Technology

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Abstract

The paper considers the technology of thermal migration for the formation of a through-layer insulation of individual crystals in the manufacture of power electronics devices. The initial Al-Si layer for the thermal migration process is formed in SiO₂ windows from the Al melt and the surface disordered Si layer dissolved in it. Selective dissolution of Si occurs when the surface of the moving wafer sequentially contacts the Al melt ribbon, where the convection flows of the melt remove the dissolved Si atoms to the melt volume. In the process, it is possible to control the thickness of the Al-Si melt formed in the SiO₂ windows. The formation of the p⁺-Si^{*}(Al) layer, which is deposited during recrystallization from the Al-Si melt during the cooling of the wafers, the high concentration of Si and the homogeneity of the Al-Si layer ensure the isotropic nature of the dissolution process and, accordingly, the faceless immersion of the discrete zone during the subsequent thermal migration process. The observed change in the polarity of the brightness contrast of the surfaces of the discrete zone and adjacent silicon in the temperature range of 1100-1130°C allows us to control the beginning of the high-temperature immersion process. The article also shows the dependence of the thickness of the Al-Si layer on the parameters of its formation process.

Keywords

Melting Al, Dissolving Si, Forming Al-Si, Recrystallization, Thermomigration

1. Introduction

When manufacturing power semiconductor devices (PSDs), the structures of which have the property of electrically blocking current of both polarities, namely such devices as thyristors, triacs with electrical or optical control, single-chip modules and forward-polarity diodes, the task of creating through-hole insulating p-walls (IW) on the wafer arises. In this case, rectifying p-n-junctions of the insulation layer are formed along the perimeter of the crystal, which connects the surfaces

of opposite sides. As a rule, the formation of insulating high-voltage p-n-junctions involves their one-sided passivation. The formation of IWs using standard boron diffusion processes is too long. In addition, such technology, due to lateral diffusion, leads to the loss of a significant part of the useful area. The solution to this problem is the use of the thermomigration (TM) process of linear zones [1-5]. In TM, the opposite surfaces of the Si wafer have different temperatures, and

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the created Al-Si liquid zone, when immersed in the volume, passes through the entire thickness of the wafer from the cooled to the heated surface. The movement of the liquid zone is accompanied by the recrystallization of the initial n-Si and the formation of a doped $p^+-Si^*(Al)$ layer, which creates an insulation p-n- junction with a breakdown voltage U_R for the device active layers.

The technology for manufacturing PSDs has varieties that are divided by the type of wafer processing, where either polished, with a high class, or ground, with a low class of surface treatment are used. Surfaces formed during grinding with coarse-grained abrasive materials provide the possibility of using aluminum diffusion processes. Such a surface of the grinded Si contains several layers: with microrelief, with cracks, and with mechanical stresses. The surface of the wafers after grinding may contain embedded particles of grinding abrasive. Cleaning the surface from such contamination requires chemical etching processes of Si, which should not cause a significant decrease in the density of surface irregularities. At the same time, such surface irregularities, which are technologically necessary, affect the course of the TM process. Accordingly, the technology under study to eliminate such an influence requires the formation of structures with a special Al-Si layer.

The task of the work is to develop a technology for forming structures with discrete Al-Si zones pre-immersed in the wafer, which would provide high-quality TM technology on Si wafers with different crystallographic orientation and different types of surface treatment. High breakdown characteristics of the formed IW insulation layer, the absence of crystallographic defects and faceting processes are what primarily determined the quality and success of TM processes during the research. The research of this work considers both the components of the technology for obtaining starting layers on the Si surface with a disturbed layer, and the physical mechanisms of the processes that occur in this case.

An important role is also assigned to the topological features of the TM pattern of a layer of crystals of a significant area, which can reach hundreds of mm^2 , where the influence of defect formation during the TM process on the yield of usable chips increases significantly, and accordingly, the requirements for ensuring conditions for minimizing the defectivity of structures during their preparation and the TM process increase.

2. Literature Review

Although previous works [6-10] consider TM processes based on the application of the studied method of creating starting discrete zones as the first stage of TM, these studies, as a rule, concern the features of the positive application of TM technology in the formation of semiconductor structures and improving their characteristics [8-10]. Works [6, 7] describes in general terms the design of the installation, where the deposition of the initial layer occurs upon contact of the

Al melt with the Si surface of the moving wafer, such as called high temperature selective wetting (HSW). However, neither the influence of the disturbed layer of the surface on the TM process nor the structural features of the formed structures are considered.

In work [11] it is shown that after immersion in the volume of silicon, the migrating zone acquires an optimal stable shape only at a certain depth, due to the reduced values of the temperature gradient in the near-surface layers at a depth of up to 40 μm . It should be added that the position about the low gradient value becomes even more complicated for a surface with a layer broken during grinding, as well as in the presence of various surface films, such as natural oxide films, residues of grinding materials, which have lower thermal conductivity compared to silicon.

When considering a ground surface, it should be noted that the thickness of the disturbed layer is proportional to the size of the abrasive grain and can be approximately determined by the formula $F = k\delta$, where for silicon $k=1.7$, and δ is the size of the abrasive grain [12].

Crystallographic defects of the disturbed surface layer cause an increase in its thermal resistance, which leads to a decrease in the heat flux and temperature gradient, and this blocks or slows down the TM process. Consideration of the features of the propagation of thermal waves on the starting and finishing ground surfaces shows that the relief surface contributes to the heating of the finishing side due to its high absorption coefficient of radiation from the heating source. Although the disturbed silicon layer has an increased thermal resistance to the transmission of thermal waves to the volume of the wafer, the heat flux from the hot surface of the silicon wafer is sufficient to form the necessary temperature gradient for the TM process. On the contrary, the starting relief cooled surface has a high resistance of the disturbed layer and a low radiation coefficient. Because of this, the heat flux from the wafer to the reactor walls (heat sink) has a low value, which complicates the formation of the temperature gradient necessary for the TM process. Therefore, in the presence of a disturbed surface layer, its local transformation or extraction within the TM layer is required.

The use of sputtered Al/Si films for TM on wafers with a high polishing class leads to the need to introduce additional annealing operations in order to saturate the film with Si atoms. Such starting layers of films are saturated with silicon atoms migrating from the near-surface layers of the Si wafer, and Al atoms in turn into the surface layers of Si. At the same time, the task of finding optimal annealing modes for the studied structures, in which critical defects would not form during the TM process, becomes important [13].

3. Materials and Methods

Variants of formed structures with initial TM layers on grinded Si wafers are shown in Figure 1. Initial Al-Si layers of samples Figure 1a and Figure 1b were formed from Al melt

on a special installation, the slider, on Si regions open in the SiO_2 film. On samples **Figure 1a**, these Si regions were opened using photolithography processes. The technological version of the structures **Figure 1b** provided for the removal of the SiO_2 film by a laser beam on an ЭМ210 scriber in CW mode in order to possibly simplify the technology.

To compare different technologies, TM processes were studied on the structures of **Figure 1c-d**, where the aluminum film was deposited using sputtering processes. On the samples of **Figure 1c**, the aluminum sputtered onto the Si wafer was left only in the pre-formed etched grooves. On the samples of **Figure 1d**, discrete zones were formed directly on the grinded surface. The thickness of the deposited metal layer was about 20 μm . The etching of the grooves was performed to a depth of 20 - 25 μm in a solution of hydrofluoric, nitric and acetic acids in a ratio of 2:8:1.

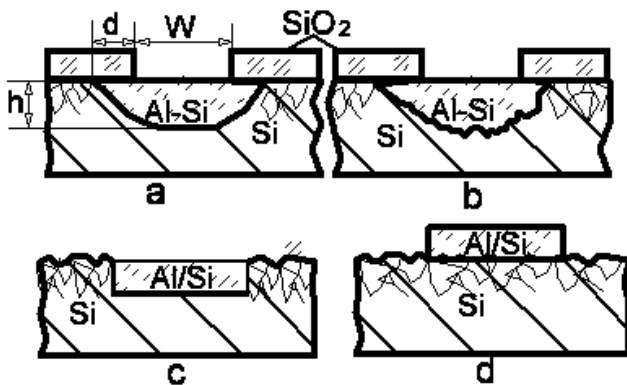


Figure 1. Types of samples of the studied Si structures during the formation of discrete zones: a, b – formation of Al-Si from the Al melt with preliminary removal of SiO_2 , where a – by liquid etching, b – by laser beam; c, d – formation of an Al/Si film by Al sputtering, where c – on a surface with Si grooves, and d – on a grinded surface of Si wafers.

Semiconductor structures of devices used in the research were usually formed according to a route that has the following main blocks of operations: cutting ingots into wafers; – grinding the wafers surface; – Al+B “drive-in” to forming flat active p-n junctions; – oxidation of the wafers; – forming windows in SiO_2 ; – forming the initial layer for TM, where one group of samples was formed from a deposited Al/Si film, and the other from molten Al; – TM operation; – annealing followed by oxidation; – Si mesa-etching – protection of the mesa-groove surface with an insulation layer. For TM, a photomask with a discrete zone width within 40-50 μm was usually used. A breakdown voltage comparison was carried out for the structures of D106 diodes and TC106 thyristors at a temperature of 20°C and a leakage current of 20 μA .

Si wafers formed for the TM process had a thickness spread of no more than 20 - 25 μm . Grinding processes were performed with abrasive powders with coarse grain M20, M14. It was possible to use wafers with a surface after cutting single-

crystal ingots followed by etching.

TM processes, where the initial layers were formed using different technologies, were performed on wafers from a monocrystal silicon ingot of the KEF-40 (111) brand. To compare TM processes on silicon of different crystallographic orientations, KEF wafers were used, for [100] with a resistivity of 36-39 $\text{Ohm}\cdot\text{cm}$, and for [111] with a resistivity of 39-42 $\text{Ohm}\cdot\text{cm}$. Variations in the thickness of the layer from the melt were obtained by changing the parameters of the deposition mode. The study of the influence of the layer thickness on the magnitude of the breakdown voltage of the device insulation was conducted for layers of 15 μm and 35 μm .

The pattern of the photomask for the TM operation is formed by connecting all the zones of different purposes, which are necessary both for forming the isolation areas of each PSD chip, and for performing certain auxiliary functions. Thus, the TM layer component in the form of a circle from the edge of the wafer is intended for leveling and stabilizing the temperature fields in this part of the wafer. The connecting zones, which are necessarily observed in the corners of the chips, combine the individual isolation zones into a single ensemble.

The slider design has a retractable graphite assembly located in a quartz tube, where annealing is carried out by an external system of IR quartz halogen lamps surrounded by a cylindrical radiation reflector. The process takes place in a vacuum $(1\div2)\times10^{-5}$ mmHg. The scheme of contacting the surface of the moving wafer with the Al melt ribbon and the features of the convection motion of the melt during the formation of Al-Si starting layers is shown in **Figure 2**.

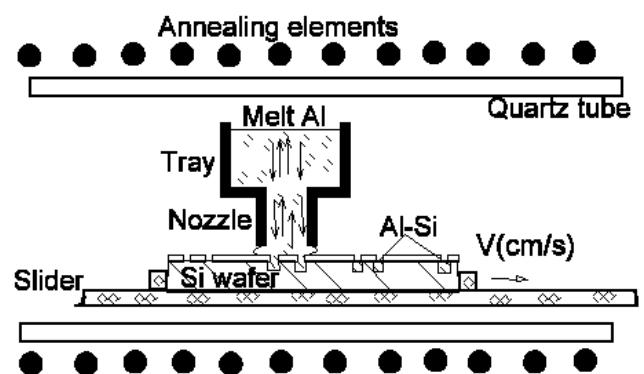


Figure 2. Scheme of HSW contacting the Al melt with the surface of the moving wafer for forming the initial Al-Si layers for the TM process.

The graphite unit works as follows. The gate - slider captures the wafer and guides it under the melt. When the wafer moves, its starting surface comes into contact with a strip of melt, which sags under the nozzle gap. A capillary connection with the melt is formed between the wafer surface and the nozzle and its interaction with open silicon areas occurs. Thus, the entire surface of the silicon wafer is pulled through the melt,

and the interaction of the aluminum melt with the surface layer of the Si wafer forms the initial Al-Si layers. Then the wafer, continuing to move, moves from the zone of contact with the melt to the control zone, where it is removed from the slider and fixed, and the slider returns to its original position to repeat the cycle. Stopping the wafer allows for visual control of the thickness of the Al-Si layer. When the next wafer is fed into the fixing zone, the previous wafer is transferred to the receiving cassette, where it is cooled.

When studying the technological capabilities, the operating temperature of the wafers varied in the range from 600°C to 900°C. During the deposition process, conditions are created for the formation of convection flows of the melt from the wafer surface to the entire mass of the tray melt. Therefore, simultaneously with the process of dissolving silicon atoms by the melt, the process of their removal by convection moving flows is implemented, where the heated part of the melt moves from the wafer surface, and the colder part - to the Si surface. Silicon, due to convection processes, enters the tray melt, where its concentration does not exceed 2...3 wt. %. In addition, the etching of the silicon wafer releases possible residual particles of the grinding powder, which rise to the surface of the tray melt with convection flows. Periodic removal of the surface layers of the tray melt implements its cleaning from contaminants.

A photograph of the external appearance of the components of the slider design is shown in Figure 3. It shows a graphite assembly protruding from the quartz tube. In the foreground is a cover for pressing Si wafers in the cassette. At the bottom of the cassette is a movable slider with grooves for gripping and moving the wafers. Behind the cassette is a tray with molten aluminum. Behind the tray is the area of removal and fixation of the wafer, where it is possible to visually control the thickness of the formed layer through the glass of the quartz tube. In this case, the dimension d is controlled (Figure 1a), which determines the width of the lateral penetration of the Al-Si layer under the oxide film. Where the width of the formed layer is determined as $W_k = W + 2d$. W is the topological width of the open silicon zone. Since the silicon dissolution process is close to isotropic, the depth of the etching groove h and, accordingly, the thickness of the starting layer can be estimated as $h \approx d$. The depth h is determined more precisely from the equation $h = kd$, where k is a coefficient determined experimentally by measuring the thicknesses h and d . The time of the slider movement back and forth is less than a minute. For the kinetic characteristics of the Al-Si layer formation process, it is convenient to use such a parameter as the reduced interaction time t_k for a Si surface plane with a side size of 1 mm, which is determined by the time of its contact with the entire mass of the melt in the tray. This time is defined as the ratio of the nozzle gap width L_D to the Si wafer speed V : $t_k = L_D/V$. The dependences of the thickness h were determined when studying the operating modes, which were corrected by changing the interaction time and annealing temperature.



Figure 3. Appearance of the graphite unit of the device for forming an Al-Si layer from an Al melt.

Carrying out TM processes required determining the dependences of the thickness of the Al-Si layer on the parameters of its formation mode, namely on the melt temperature and the contact time t_k . In this case, the layer thickness was determined by means of post-operative control of the depth of the groove formed on the surface of the Si wafers after selective removal of the Al-Si layer. The concentration of silicon atoms in the melt of the Al-Si discrete zone before cooling the wafers was determined by their temperature in accordance with reference data.

The study of the structure of the Si surface layers after the creation of immersed Al-Si discrete zones was carried out by forming ball sections according to standard methods. For this, the Al-Si layer is first selectively removed from the wafer surface, and a recess is formed using a ball, where the formed section is checked for the presence of surface regions of Si p-type conductivity by the formation of optically colored layers and studying the contact voltage-current characteristics in this region.

The formed structures of Figure 1 were used in the next TM operation, which was carried out in a vacuum $(1 \div 2) \times 10^{-5}$ mm Hg at a temperature of 1180°C. The study of TM immersion processes included the study of the change in the contrast of the radiation brightness of the Si wafer surface, both of the deposited Al-Si layers and of the adjacent Si regions, depending on the temperature when it increases in the range of 1000-1250°C. Such visual control was carried out through the illuminator glass in the wall of the TM chamber. Annealing on TM installations was carried out using resistive elements placed in the center of a hollow graphite pyramidal pedestal on which the wafers were installed in a vertical position. TM processes were carried out on two installations with different temperature gradients of 50 and 20°C/cm. In addition, for comparison, TM processes were carried out on installations with induction annealing in a nitrogen gas environment. Carrying out the TM process on samples with a deposited film (Figure 1c) provided for additional annealing at a temperature of 580°C to saturate the film with silicon atoms by increasing

the corresponding time interval by 30 min.

The plane along which the TM immersion occurs was determined on a SUPRA 40WDS scanning electron field emission microscope by studying the shape of the side surface of the section of the epitaxial Si*(Al) layer formed during TM. The research methodology is described in [3], where visualization of the shape of the near-surface side surface of the Si(Al) isolation region was achieved by its selective chemical etching during the formation of a mesa-groove during the preparation of the Si wafer surface for the subsequent passivation operation. Epitaxial Si*(Al) has a higher etching rate relative to the n-Si of the original wafer, which allows us to detect the shape of the Si*(Al) side surface [3]. Since this method is destructive, when studying the shape of the lateral surface, as a rule, generalization is made for several samples of the same type.

4. Results

TM processes were successful on samples of three types of initial layers, which are shown in Figure 1a, 1b and 1c, respectively. Although the manufacturing technology of samples 1b was successful, the laser beam processing installation used does not have sufficient precision parameters for adjusting the wafer movement necessary to meet the technological requirements for forming the TM layer, therefore, this method has not yet been further implemented. The data in Table 1 compare TM processes on samples 1a with initial layers formed from the melt, and samples 1c with a layer formed by a film deposited in grooves. The features given in the table show the advantages of the technology for forming an Al-Si layer from an Al melt.

Table 1. Comparison of technological features of different methods for forming starting layers for the TM process.

Forming method	
Vacuum sputtering	Selective deposition from the melt
Technological features	
Stable TM directions. On silicon (111) all; on (100) only two: [011] and [0 $\bar{1}$ 1]; on (110) only one [011].	Zones of any orientation migrate stably on the (111), (100), (110) wafers.
The need for preliminary annealing before TM immersion of structures	Preliminary annealing before TM immersion is absent.
Technological imperfection of TM due to the possibility of defects formed during sputtering and pre-operational annealing.	Simple, universal TM technology with no defect formation.
The breakdown voltage U_R is lower. The breakdown locations are located randomly along the boundary of the insulation layer, which is associated with the formation of structural defects.	The breakdown voltage U_R is higher. The breakdown points are located near the corners of the chips, which is due to the design feature of the diffusion structures.
Higher aluminum consumption when sputtering the entire wafer surface	Lower aluminum consumption due to selectivity of layer formation.

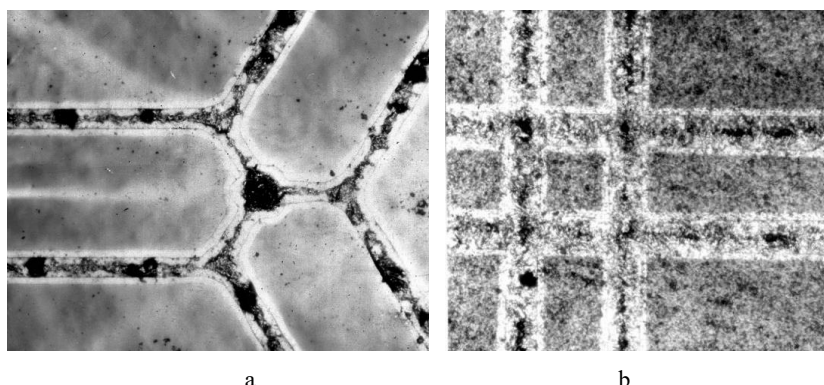


Figure 4. Appearance of the Al-Si layer formed in the windows of the SiO₂ film from the Al melt on Si wafers with different types of surface treatment: a) hexagonal chip, polished surface; b) quadrangular chip, grinded surface.

The formation of initial layers from the melt allows to ob-

tain a high yield on large-area chips on silicon wafers of different crystallographic orientation. Although such technology

is primarily necessary when using wafers with a broken layer, the possibility of its application does not depend on the state of surface treatment.

The photo in Figure 4 shows structures with an Al-Si layer formed from molten Al on Si wafers with different types of surface treatment. It also shows the topological features of combining TM discrete zones of individual chips into a single structure in the region of the corners of hexagonal and tetragonal crystals of semiconductor devices.

The bright edge of the TM layer strip corresponds to the part of the Al-Si layer formed under the oxide mask, the width of which in Figure 1a is indicated by the letter d.

The dependences of the thickness h of the Al-Si layer formed on silicon (111) wafers on the process parameters, namely on the contact time t_k and the temperature T , are shown in Figure 5. Formation of the initial layer at a temperature of 780°C and a thickness h within 18 μm for Si(111) and 15 μm for Si(100) allow obtaining reliable TM processes and quality characteristics of the insulating TM layer, are technologically convenient and were taken as optimal. The values of the thickness h , which were obtained for the grinded surface, with corrections for the surface relief, were also applied to wafers with a polished surface.

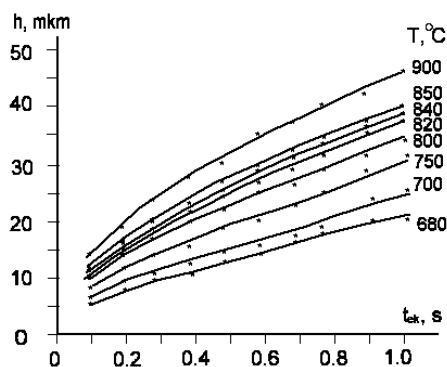


Figure 5. Dependences of the thickness h of the Al-Si layer formed on silicon (111) wafers with a disturbed layer on the parameters of the processing mode: contact time with the melt t_k and melt temperature T .

Studies on the formed spherical recesses of the conductivity type of the near-surface Si layers under the deposited Al-Si layer showed the presence of a p^+ -Si layer with a thickness of $h_p \approx 1 \mu\text{m}$. Diffusion processes take part in the formation of the p^+ -layer, but at the studied temperature of 600 - 900°C the diffusion coefficient is quite low. Therefore, the formation of such a layer occurs due to the processes of recrystallization of silicon from the melt during its cooling. The structural arrangement of this recrystallized layer is shown in Figure 6a. Reference data on the equilibrium silicon content in the melt for the working and crystallization temperatures allow us to determine the amount of silicon that is released to participate in the recrystallization process, which allows us to calculate the thickness of the formed layer for slow equilibrium cooling.

The calculation of the p^+ -Si layer thickness was carried out for a layer of 20 microns depth, with the formation of structures in one case at 780°C (28% silicon) and in the other at 900°C (37% silicon). Thus, the melt of the Al-Si layer at a temperature of 780°C according to the phase diagram has a silicon concentration of 28 mas. %. When the composition is slowly cooled in the solid phase at 577°C, the Si-Al zone with 12% silicon and a crystallized p^+ -Si*(Al) layer remains, where silicon will be about 99.95 mas. % with the remainder of aluminum. The calculated values of the p^+ -Si* thickness are $h_p \approx 2.9 \mu\text{m}$ for the temperature $T=780^\circ\text{C}$ and $h_p \approx 4.5 \mu\text{m}$ for $T=900^\circ\text{C}$. The relatively rapid cooling of the Al-Si melt used in practice causes the calculated value of the p^+ -Si* thickness to significantly exceed the experimentally obtained one. Calculations of the residual Si in the solid solution during the observed cooling of the melt with a temperature of 780°C show that when a p^+ -Si* layer with a thickness of $h_p=1 \mu\text{m}$ is formed, about 20 mas. % Si remains in the solid phase Al(Si)-Si. Of which 12 mas. % Si is a stoichiometric component of the formed solid phase, and 8 mas. % Si is released as Si precipitates in the Al(Si)-Si solid solution.

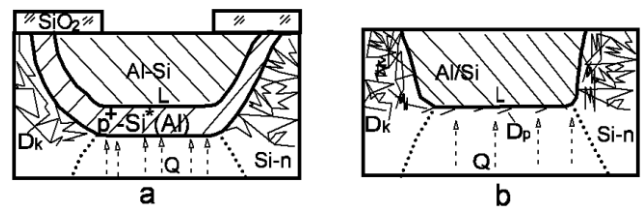


Figure 6. The structure of the initial layers depending on the method of their deposition: a) Al-Si formation from Al melt; b) Al/Si film deposition on the surface of the wafer with grooves.

Electron microscopic studies of the lateral shape of the cross-section of the through-hole region of the TM layer of epitaxial Si*(Al) showed that at a depth h , which determines the thickness of the initial Al-Si layer, a narrowing of the epitaxial Si*(Al) layer is observed. Such a narrowing, which is marked L in Figure 6, corresponds to the surface where TM immersion begins. The immersion of the liquid zone begins from the surface of the initial Al-Si layer most deeply embedded in Si, where its width has the value W_L . The wider surface side part of the Al-Si layer, which was formed under the mask, is fenced off from the volume of the Si wafer by the disturbed layer D_k , and this layer D_k at the TM stage blocks the possibility of direct vertical immersion of this part of Al-Si. From this it is possible to conclude that although on the crystal surface the width of the Al-Si layer is determined as $W_k=W+2d$, the width of the discrete zone, where its TM immersion begins, is determined by the width W_L - the bottom narrowing of Al-Si on the initial structures, which can be approximately determined by the given value W of the topological width of the TM region (Figure 6a). The surface structure L for the samples shown in Figure 6a and Figure 6b was studied using optical

microscopy after removing the layer of discrete zone with aluminum. The samples of Figure 6a with Al-Si formation from the Al melt have a polished surface L, and the samples of Figure 6b with Al/Si film deposition have a segmented surface, where the segments are formed by Si planes of different crystallographic orientations and have the appearance of “rows of tiles”. That is, the etching of Si in the case of Al-Si samples is isotropic and polishing, and in the case of samples with Al/Si film deposition it is anisotropic. The transition layer D_p , which is formed during annealing of the deposited Al/Si film at its interface with the single-crystal silicon of the wafer, is shown in Figure 6b. This D_p layer is largely responsible for the occurrence of the described anisotropic etching of such samples.

Control of the I-V characteristics of the insulation layer of the studied samples made of silicon of different crystallographic orientation gave the following results. For zones with a thickness of 18–20 μm , the average value of the breakdown voltage was 1675 ± 100 V for (111), and for (100) - 1750 ± 90 V. That is, for structures (100) the UR values are larger, and the spread is smaller. Similar patterns were obtained for the anodic and cathodic transition of the studied devices. For zones of increased thickness of 35 μm , the average value of the breakdown voltage for Si (100) was 1521 ± 107 V. When comparing the I-V characteristics of samples manufactured using different technologies for forming the initial layer, the following results were obtained. The average values of the breakdown voltage of the insulation layer for the Si(111) samples with sputtered zones were 1055 ± 400 V, and for the samples with zones formed from the melt - 1550 ± 340 V. For zones of increased thickness of 35 μm Si(111) the average value of the breakdown voltage of the insulation layer was 1198 ± 267 V. The structures with sputtered zones have a smaller breakdown value, and the breakdown locations are located along the insulation layer randomly. The structures of the devices, where the initial layer is formed from the melt, have relatively higher breakdown voltage values, while the breakdown occurs in topologically defined places, namely in the area of the corner roundings of the chip insulation layer.

When carrying out the high-temperature TM process, the most important stage is the immersion of liquid zones in silicon. And the success of this immersion process can be monitored by monitoring the change in the contrast of the brightness of the surfaces of the discrete zone and the adjacent silicon matrix. In the temperature range of 1100 - 1130°C, a noticeable change in the relative brightness of the zone and the matrix is observed. If at temperatures of about 1000°C the zone looks brighter against the background of a dimmer matrix, then with increasing temperature and, accordingly, with increasing percentage of silicon in the melt of the zone, the brightness of the zone and the matrix initially becomes the same, and then the brightness of the zone decreases against the background of a bright matrix. Which may indicate a corresponding change in the direction of the tangential component of the temperature gradient near the zone, which accompanies

the immersion process. At the edges of the zone, films of recrystallized silicon are formed and further increase on both sides, moving towards each other. After their “closing”, the zone is already submerged and migrates in the middle of the silicon wafer in the direction of the normal component of the temperature gradient.

A similar pattern was observed both in installations with resistive annealing with different temperature gradients and with induction annealing in a gas environment. Such contrast control allows determining the success of the beginning of the TM immersion process, which is the key to the success of the TM process as a whole.

5. Discussion

The absence of TM immersion processes on samples with an Al/Si film deposited directly onto the polished surface of the plate (Figure 1d) can be explained by the presence of a disturbed layer under the deposited film, which blocks TM immersion processes in the discrete zone region.

Samples with Al/Si (Figure 1c) have a smaller electrical breakdown value compared to samples with Al-Si (Figure 1a), and the breakdown sites are located along the boundary of the discrete zone. Such relative differences between samples with Al/Si (Figure 1c) may indicate the occurrence of defects during their preparation and TM. A layer of natural oxide may remain between the matrix and the deposited film on these samples, and sometimes contamination may get in. Such shortcomings have a negative impact on the immersion process. Attempts to improve the conditions for the formation of deposited zones and optimize their annealing deserve attention. Improvements in the insulation characteristics of the IW can also be obtained with a relatively long annealing after TM [8]. For zones formed from the melt, such improvements are usually more significant. On the contrary, the success of TM of the initial Al-Si layer formed from the melt on Al-Si samples (Figure 1a) is explained by their structural readiness for the TM technological process, including on polished Si wafers. It is important to note that the liquid-phase formation of discrete zones is adequate to the TM operation, which is also liquid-phase. The main ordering of the structures before the next TM operation and their positive impact are determined by the following: removal of the disturbed Si layer by the Al melt; creation of a high concentration of uniformly distributed Si atoms in the formed recessed Al-Si layer; formation of a recrystallized p^+ -layer of $\text{Si}^*(\text{Al})$ upon cooling; absence of faceting processes of a discrete zone, absence of degradation associated with the formation of structural defects with a smaller electrical breakdown value.

Since TM immersion of the liquid zone occurs along the frontal plane L (Figure 6), it is important to consider the structural features of the formation of the p^+ -layer precisely at this location. The formation of the Al-Si layer in bulk Si allows you to get rid of the influence of both foreign compounds and impurities, namely contaminants similar to natural oxide films,

and crystallographic disorders associated with surface treatments. This is confirmed by the formation of a high-quality high-voltage p-n junction based on the p^+ -layer of recrystallized Si. In work [14], an anodic p-n junction of a power diode structure was formed on structures with a similar p^+ layer formed from the Al-Si melt.

Zones formed by different methods on different samples are immersed synchronously, which is confirmed by the synchronous change in brightness contrast on Al-Si and Al/Si samples. But if the sputtered Al/Si zone – according to the generally accepted theory [15] – undergoes faceting, then the zones formed from the Al-Si melt, while they are not oriented, migrate stably without faceting. The explanation here is as follows. In sputtered zones, with a non-uniform distribution of impurities, the dissolution of the Al/Si layer, according to the state diagram, begins at 577°C in local areas with a minimum silicon concentration. Such local non-uniform formations of the liquid phase of the zone and cause anisotropy of the beginning of TM immersion, which provokes the possibility of the formation of facets. On the contrary, the liquid-phase formation of Al-Si zones with the creation of a recrystallized p^+ -layer corresponds to isotropic dissolution of Si, which is easy to verify by removing the formed Al-Si zone in a liquid selective etchant and obtaining a groove with smooth walls in its place. This confirms the absence of processes of local non-simultaneous nucleation of the liquid phase at the beginning of TM immersion of the zone from the Al-Si layer. That is, the formation of the melt in the TM process on samples with an Al-Si layer is homogeneous and does not have local areas of liquid phase formation at relatively lower temperatures.

Increasing the thickness of the liquid zone to 35 μm accelerates the TM process itself, but the immersion of more massive zones, which are at the same time thicker and wider, leads to an increase in the defectivity of the TM layer, which causes a decrease in the breakdown voltage of vertical transitions of SR structures. This significant decrease is not corrected by subsequent annealing, so thickening of the zones is unacceptable.

Thus, the technology of forming discrete zones from the melt at a temperature of 720–800°C, where a zone with a high silicon content is formed during rapid cooling and a high-quality recrystallized p^+ -silicon layer is created, is consistently successful. Accordingly, such technology does not require preliminary orientation of the zones relative to the $\langle 011 \rangle$ direction, and the shape of the zones can be arbitrary without reducing the breakdown voltage of SR transitions. At the same time, the structure of the unpolished surface of the silicon wafer is not an obstacle to the formation of high-quality devices.

6. Conclusions

The emergence of the advantages of the considered technology is due to the initial formation of a layer of silumin melt and its subsequent crystallization with the formation of an in-

itial layer of discrete Al-Si zones. The dissolution of the disturbed layer of the grinded surface of the Si wafers occurs at a temperature of 600–900°C in the Al melt, where convection flows are present. The Al-Si melt layer is formed in the windows of the SiO_2 film of the moving wafers during the contact interaction of Si with the Al melt. When the structures are cooled, solid-phase discrete Al-Si zones with a high concentration and uniform distribution of Si atoms are formed. A thin layer of crystallized p^+ -Si layer doped with Al is also formed. Such a structure ensures the high-quality flow of the TM immersion processes and the formation of an insulation layer with high breakdown voltages. The beginning of the successful process of high-temperature TM immersion was controlled by changing the polarity of the relative contrast of the brightness of the surfaces of the discrete zone and adjacent silicon in the temperature range of 1100–1130°C.

7. Recommendations

The use of the developed HSW technology for the formation of TM zones is more adequate compared to the deposition of films and their annealing.

It is recommended to use the control of the change in brightness contrast to determine the moment of immersion of the zones.

In the production of PSD chips using TM technology, the use of silicon (100) has a number of advantages over the traditional (111).

Abbreviations

IW	Through-Hole Insulating P-Walls
PSD	Power Semiconductor Devices
TM	Thermomigration
Al/Si	Film Formed by Vacuum Deposition
Al-Si	Layer Formed by Dissolving Silicon of a Single Crystal Wafer in Aluminum Melt
$p^+\text{-Si}^*(\text{Al})$	The Aluminum-Doped Layer is Formed During the Recrystallization Process from the Al-Si Melt
U_R	Breakdown Voltage

Author Contributions

Vitalii Kravchyna: Conceptualization, Investigation, Formal analysis, Writing – review & editing

Oleksii Polukhin: Investigation, Data curation, Methodology, Writing – original draft

Conflicts of Interest

The authors declare no conflicts of interest.

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