Journal of Electrical and Electronic Engineering
2025, Vol. 13, No. 1, pp. 82-91
https://doi.org/10.11648/j.jeee.20251301.17

Research Article

A High-Resolution Non-Volatile Floating Gate Transistor Memory Cell for On-Chip Learning in Analog Artificial Neural Networks

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Abstract

This paper proposes a high-resolution non-volatile memory cell design that addresses the most substantial limitations associated with the effective implementation of analog long-term memory storage solution. Prior research efforts often suffer from limited resolution, hindering their ability to accurately represent fine-grained weight adjustments required for effective learning in analog neuromorphic systems. This work effort has been channeled toward crafting conductive circuit designs using 90 nm complementary metal-oxide semiconductor technology for on-chip learning applications in analog neuromorphic systems. The operational mechanism of the cell involves the storage of charge on the floating gate of the NM0 transistor. The writing process is accomplished through hot-electron injection, while the erasure of stored information is executed via gate oxide tunneling. An advantageous feature of this cell is its capability to facilitate simultaneous reading and writing of data. The reduction of errors that may arise due to oxide mismatch or charge trapping is achieved through feedback control incorporation during the writing phase. The memory reveals clear synaptic behavior characteristics in storing and retrieving analog information reliably including, good memory cell resolution, good charge retention rate, reliable operation in noisy environments, and high resolution with faster learning with a power consumption of 1.06 μW and an output current of 10 μA under a typical operating voltage of 1 V. This strategic implementation enhances precise and reliable weight updates within neuromorphic analog artificial neural networks, which is essential for ensuring accurate on-chip learning outcomes as well as minimizing power consumption.

Keywords

Analog Artificial Neural Network, Floating Gate Memory, On-Chip Learning, Complementary Metal-Oxide Semiconductor

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Received: 2 February 2025; **Accepted:** 17 February 2025; **Published:** 27 February 2025

1. Introduction

Artificial Intelligence (AI) systems have driven significant advancements in the hardware and software domains. Analog Artificial Neural Networks (AANNs) have emerged as a promising tool for achieving energy-efficient and high-speed AI solutions. However, a major drawback to realizing AANNs is the lack of reliable on-chip learning analog memory cells for enabling real-time adaptation and dynamic behavior [1]. For example, Zhang *et al*. proposed a capacitive storage memory structure with clock refresh to enable efficient accumulation [2]. This structure suffers however from volatility and limited resolution. Also, Pechmann *et al*. introduced a multi-bit digital memory block that uses resistive cells for weight and bias storage in an embedded and distributed manner [3]. This approach offers programming flexibility and reduced power consumption but exhibits low endurance. Moreover, integrating [2] and [3] directly into AANNs poses challenges due to mismatch issues and process variations. Furthermore, Huang *et al*. highlighted that current AI, primarily based on AANNs, faces two critical challenges: high energy consumption and limited ability to generalize knowledge and adapt to changes [5]. These challenges open up new perspectives for implementing neuromorphic systems using analog devices. Floating Gate (FG) transistors exhibit an inherent aptitude for retaining non-volatile analog memory [4]. Likewise, Haensch *et al*. indicated that material properties significantly influence AANN system-level characteristics, including speed, power, and classification accuracy [6]. They reviewed the cross-bar-based computer in memory, considering both digital and analog memory while emphasizing co-design principles. Furthermore, Aguirre *et al*. investigated the use of memristors in neural network hardware [7], stipulating that memristors have potential low-resolution applications in medical informatics. On the same path, Chen *et al*. proposed a fully analog hyperbolic tangent function (tanh) implementation using phase-change memory [8]. These analog-memory-based AANN architectures are compatible with on-chip learning neural networks, offering effective means for implementing neurons based on analog memory. Additionally, Won *et al*. explored a novel approach to multi-neuron connections using multi-terminal FG memristors [9]. The study allows memory charging and discharging using horizontally distant multiple electrodes. Similarly, Winterfeld *et al*. proposed a MemFlash cell based on resistive switching [10]. Unlike memristive devices, the MemFlash cell is purely an electronically based switching device with FG transistors as key elements, exhibiting memristive switching behavior. Also, Han *et al*. proposed a digital method utilizing an FG transistor-based in-memory computing chip [11]. They achieve equivalent precision and high parallelism as Naqi *et al*. who developed an electronic synaptic device based on a synthesized memristor array [12], demonstrating memory performance, including retention and clear synaptic functions. Subsequently, Xu *et al*. unveiled a novel photonic activation function for neural networks that utilizes a non-volatile opto-resistive memory switch [13]. This memory could have applications in analog networks, enabling flexible optical signal processing. Recent research has explored FG transistors for on-chip learning in AANNs, offering several advantages, including non-volatility, high density, and excellent programmability. Paliy *et al*. suggested a 180 nm Complementary Metal-Oxide Semiconductor (CMOS) single-poly technology platform based on analog vector-matrix multiplier architectures that use in-memory computation with FG multi-level non-volatility for analog neural network-integrated circuits [14], investigating accuracy through system simulations and temperature-dependent stored weights.

However, existing mentioned memory cells often suffer from limited resolution, hindering their ability to accurately represent fine-grained weight adjustments required for effective learning in AANNs. This work effort has been channeled toward crafting conductive circuit designs using 90 nm CMOS technology for on-chip learning AANNs, introducing an analog memory architecture using high-resolution non-volatile FG transistors to address the mentioned challenges. This memory offers several advantages for on-chip learning, including nonvolatile analog storage, high resolution, large dynamic range, on-chip simultaneous reading and writing operations, low power consumption with compact size, and compatibility with standard CMOS processing. By leveraging these advantages, this work aims to develop a memory cell capable of facilitating precise, persistent, and energy-efficient weight updates in AANNs. This design incorporates components such as an operational amplifier, which plays a pivotal role in the memory writing phase, transistors, and an adder circuit, which are integral to the weight modification synaptic process. This research contributes significantly to AANNs by paving the way for efficient and robust on-chip learning mechanisms, opening new avenues for developing intelligent systems in medical informatics.

The implemented memory in this work reveals clear synaptic behavior characteristics in storing and retrieving analog information reliably including, good memory cell resolution, good charge retention rate, reliable operation in noisy environments, and high resolution with faster learning with a power consumption of 1.06 μW and an output current of 10 μA under a typical operating voltage of 1 V. This strategic implementation enhances precise and reliable weight updates within neuromorphic analog artificial neural networks, which is essential for ensuring accurate on-chip learning outcomes as well as minimizing power consumption. This paper is organized as follows: the methodology used in designing the memory cell circuit block is presented in Section 2. Section 3 highlights the simulation results of the memory. Section 4 then focuses on the interpretation and validation of the obtained results. Finally, a brief conclusion and perspective for further studies are given in Section 5.

2. Materials and Methods

Although FG transistors are widely recognized as memory components [15, 16], their application in silicon neural networks has been limited due to the lack of an effective bidirectional data-writing mechanism. Writing data involves moving charge carriers through the silicon dioxide-insulated gate of an FG transistor. Although Fowler–Nordheim tunneling [17] and hot-electron injection are established techniques for this process, they have historical challenges. This work utilizes floating node connections of isolated n-type and p-type Metal–Oxide Semiconductor Field-Effect Transistor (MOSFET) tunneling to extract electrons from the FG by applying positive high voltages to a lightly doped n-type CMOS transistor (with an impurity concentration of approximately $10^{17}/cm^3$) to create an environment where an n+ implant exists. Electrons are introduced into the FG through bidirectional tunneling. However, this method requires either dual polarity high voltages or a single polarity high voltage. Both options have drawbacks: dual polarity results in a low negative voltage compared to the substrate potential, while single polarity lacks simultaneous memory reading and writing support. Another approach is hot-electron injections [18] in n-channel transistors requiring drain and gate voltages to exceed 3.1 V. This leads to high channel currents and power consumption unsuitable for on-chip learning in AANNs.

In contrast, rather than directly modifying a conventional n-type MOSFET channel, we enhance its injection rate through the introduction of a base implant by increasing PMOS substrate doping to reach V_{tun} of 6 V in an unprogrammed state, allowing sub-threshold channel currents at gate voltages sufficient to capture injected electrons. Selecting an injection transistor drain voltage of 5 V, ensures that the writing rate remains unaffected by minor variations in drain voltage, even though the drain breakdown voltage is approximately 7.25 V. The proposed analog memory cell in Figure 1 utilizes floating gate transistors and a comparator circuit coupled to an adder to achieve non-volatile weight storage and accurate weight updates without constant refresh. This paper assumes the following methodology for the erasing, writing, and reading processes: Firstly, the memory cell is reset to its initial state before writing a new weight value. A positive high-voltage, V_{tun} is applied to the control gate of the FG. This voltage induces Fowler-Nordheim tunneling, removing electrons from the FG. As electrons are removed, the output voltage, V_{out} approaches ground level. After erasure, the V_{tun} voltage is lowered, disabling the tunneling current and preserving the erased state. Secondly, in the memory writing phase, the target voltage obtained from weight adjustment in the adder circuit is set by applying the desired memory voltage, V_{in} to the non-inverting input of the comparator, A. The comparator is enabled, causing its output to adjust the drain voltage of the injection transistor, PM1 to a high level. The high drain voltage of PM1 generates a strong electric field, allowing electrons to be injected into the FG. As electrons are injected, the output voltage, V_{out} of the FG increases. When V_{out} surpasses the target voltage, V_{in}, the comparator changes its output state, lowering the drain voltage of PM1 to the ground. The comparator feedback ensures that V_{out} remains at the desired value V_{in}, as modeled by equation (1). Finally, the stored weight value is obtained by directly measuring the output voltage, V_{out} of the FG through a feedback capacitor C_i during the reading process. Importantly, the non-destructive read operation is ensured by the charge stored on the feedback capacitor which maintains unchanged the stored weight.

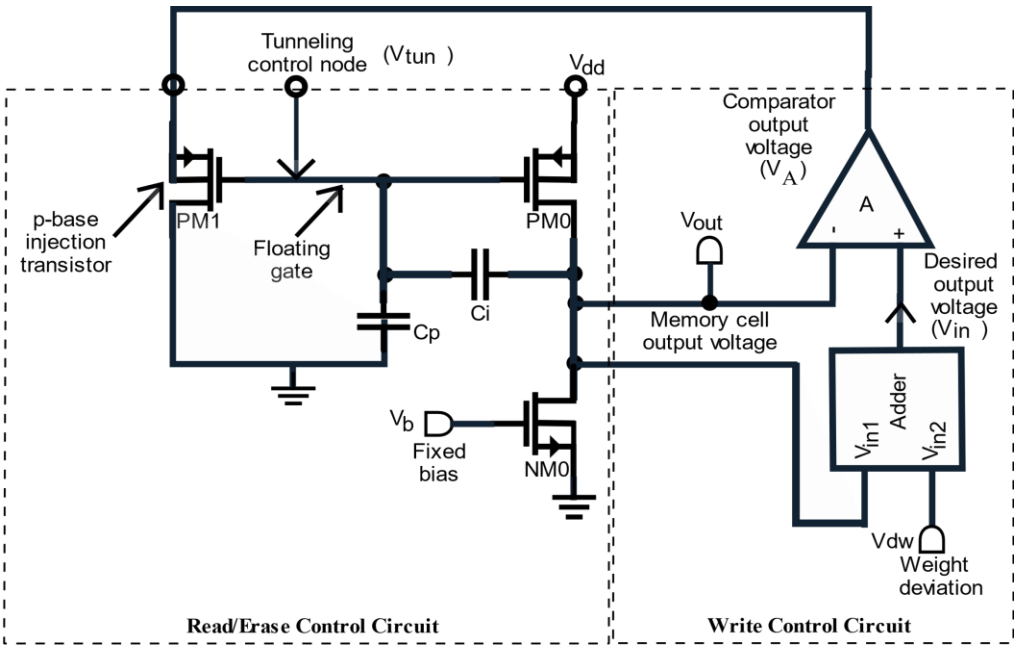

Figure 1. *Analog memory cell circuit.*

$$V_A = \begin{cases} 0 \; if \; V_{out} < V_{in} \\ V_{in} \; if \; V_{out} \geq V_{in} \end{cases} \quad (1)$$

Furthermore, transistor NM0 depicted in Figure 1 is used for biasing. The amplifier formed by NM0 and PM0 drives the output node. Utilizing subthreshold channel currents allows for rail-to-rail output voltages and ultra-low power consumption. Transistor, PM1 facilitates hot-electron injection. The floating gate voltage must be maintained between 5V and 6V, requiring a supply voltage of 6-7 V to achieve reasonable injection rates. Capacitor C_p is the primary parasitic element, coupling from Ci to the ground for attenuating undesired signals. Additionally, this capacitor is intentionally used to fine-tune the frequency response of the memory. Additionally, during the memory writing phase, electron injection causes V_{out} to slew upwards, at a rate set approximately by equation (2). The term dV_{out}/dt represents the output voltage rate of change, V_{out} over time, essentially how quickly the voltage increases during the writing process. I_{inj}, the injection current flows into the FG and causes the output voltage to rise. C_i represents the input capacitance, which measures how much charge the FG can store. This equation establishes a direct relationship between I_{inj} and the rate of change of V_{out} during the writing process. The rate at which the memory cell is written is adjusted by controlling the injection current I_{inj}.

$$\frac{dV_{out}}{dt} = \frac{I_{inj}}{C_i} \quad (2)$$

Moreover, each weight in the AANN is represented by a specific voltage level stored in the analog memory. The weight update mechanism involves changing the voltage stored in the memory cell, reflecting the weight adjustments dictated by the backpropagation algorithm which calculates the amount of change needed for each weight based on the error signals and the learning rate. These updated weights correspond to the desired output voltages of the memory cell, obtained by adding the existing weight values, V_{out}, (corresponding to the actual output voltages of the memory cell) to the calculated weight deviation, ΔV_{dw} as in equation (3).

$$V_{out}(t+1) = V_{out}(t) + \Delta V_{dw} \quad (3)$$

The proposed analog memory cells underwent testing in controlled conditions. An external voltage source was employed for memory erasure, while an LM324 amplifier facilitated memory writing with the capacitance of feedback capacitor C_i chosen as 1 pF. This value represents a trade-off between speed and accuracy of the writing process. Optimal resolution on-chip learning applications under development utilize conventional lightly-doped drain high-voltage transistors presented in Table 1 to select memory cells for erasure. These transistors have high breakdown voltage, allowing them to handle high voltages required by the erasing process.

Table 1. *Transistor dimensions for the memory block.*

Transistor	Type	With (η m)	Length (μm)
NM0	NMOS	120	1.16
PM0	PMOS	120	0.465
PM1	PMOS	120	0.465

3. Results

3.1. Voltage Characterization

This section presents the comprehensive characterization results of the analog FG transistor memory cell output voltage behavior as depicted in Figure 2 to Figure 5. We systematically investigated the memory cell's response to variations in weight deviation voltage, focusing on key performance metrics including programmability, resolution, retention characteristics, and noise immunity.

First, the analog cell memory's voltages are depicted in Figure 2, revealing how the desired memory voltage, V_{in}, the comparator output voltage, V_A, and memory output voltage, V_{out}, respond to changes in the weight deviation, V_{dw}. V_{in}, V_A, and V_{out} are represented in black, green, and blue, respectively. The output voltage shows a desirable linear relationship with the weight deviation as required for accurate analog weight representation. A unity voltage gain is obtained between V_{out} and V_{in} for positive weight deviations, while the gain is approximately 0.96 for negative weight deviations. Thus, indicating significant memory cell sensitivity to weight updates.

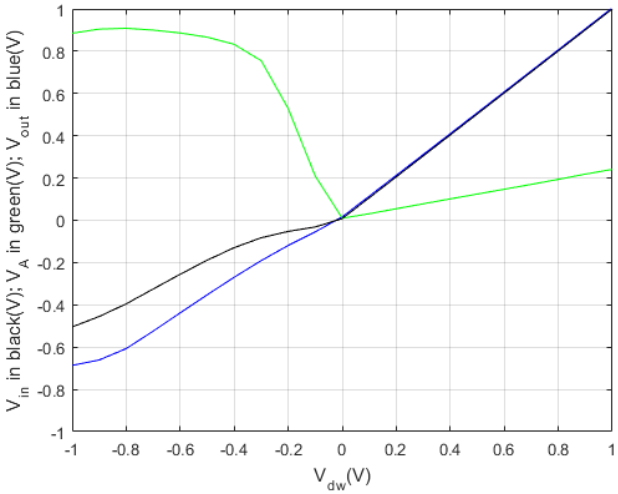

Figure 2. *Voltage responses (V_{in} in black, V_A in green, and V_{out} in blue) versus weight deviations.*

Secondly, a scatter plot with Q_{inj} on the x-axis and V_{out} on the y-axis is depicted in Figure 3, showing a linear relationship between injected charge and output voltage. This linear relationship with the slope steepness of 98.8 (close to the ideal value of 100) indicates good memory cell programmability. Furthermore, the small spacing between points on the line suggests good memory cell resolution with some slide degree of noise, allowing precise weight adjustments.

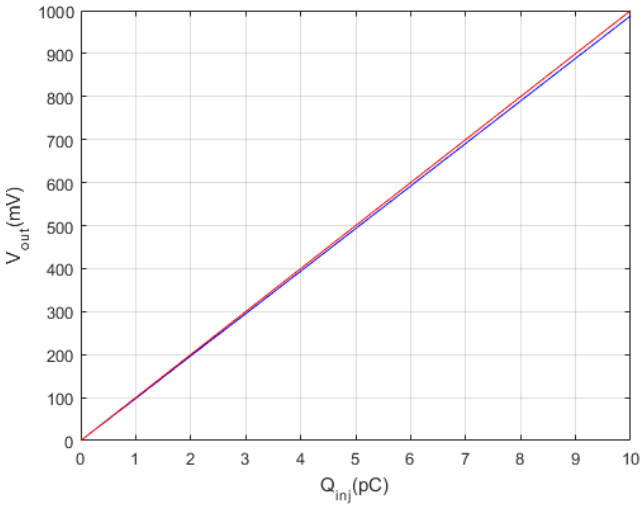

Figure 3. *Programmability and resolution characteristics.*

Thirdly, Figure 4 shows a line plot with Time on the x-axis and Vout on the y-axis, demonstrating how the output voltage decays over time after an initial charge is injected. The slope of -0.0005 (close to the ideal value of 0) with a relatively slow decay in Vout over time indicates a good charge retention rate. The charge-long retention time proves that long-term storage is desirable for AANNs.

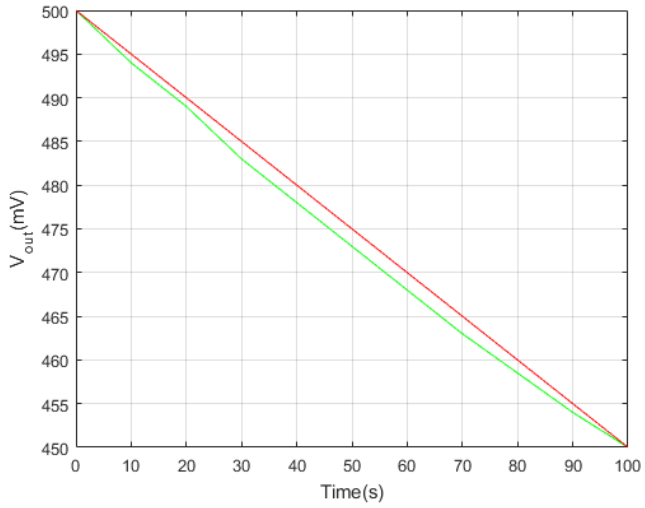

Figure 4. *Retention characteristics.*

Finally, Figure 5 depicts a plot displaying the output voltage as a function of the noise amplitude applied to the memory cell. This plot shows an approximately 10 % increase in Vout as noise amplitude increases, with a maximum noise amplitude tolerance of 100 mV. The noise amplitude is within the tolerance range of the memory cell, indicating reliable operation in noisy environments.

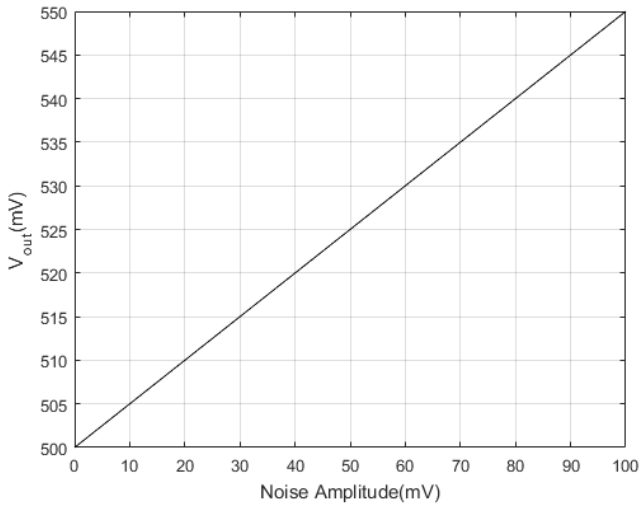

Figure 5. *Noise immunity characteristics.*

3.2. Memory Performance

This section delves into the memory cell's comprehensive performance analysis, exploring its injection efficiency, reading characteristics, memory accuracy, and writing error rate, as depicted in Figure 6 to Figure 9. This multifaceted analysis provides insights into the cell's abilities for storing and retrieving analog information, paving the way for its future integration into complex neuromorphic systems.

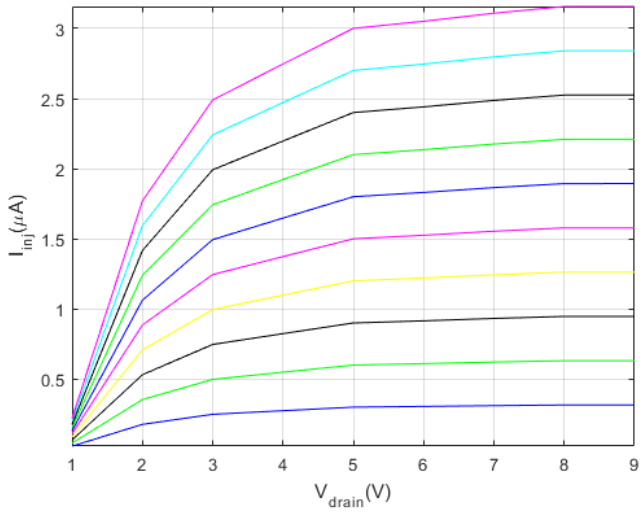

Figure 6. *Injection efficiency.*

The injection efficiency is depicted in Figure 6, illustrating multiple curve plots of I_{inj} versus V_{drain} for different V_{gate} values. Each curve shows a roughly exponential increase in I_{inj} as V_{drain} increases with some degree of linearity before the saturation regime indicating good injection. As V_{gate} increases, the curves shift upward with steeper slopes, implying higher gate voltages lead to higher injection currents at the same drain voltage. This plot demonstrates the impact of the gate voltage on the device's injection efficiency.

Furthermore, the reading characteristic of the analog cell memory is depicted in Figure 7, illustrating multiple curve plots I_{drain} over time for different V_{dw} values. This plot shows a slight increase in I_{drain} with increasing V_{dw}, demonstrating the analog memory cell takes a maximum of 1 s to memorize the written voltage. This is a crucial feature for understanding device behavior within an AANN.

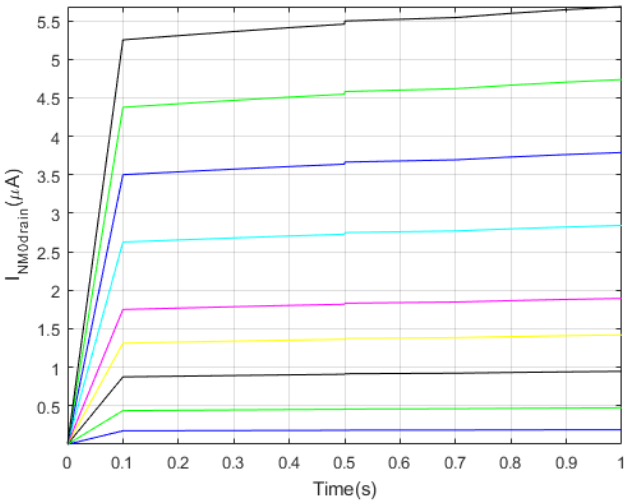

Figure 7. *Reading characteristics.*

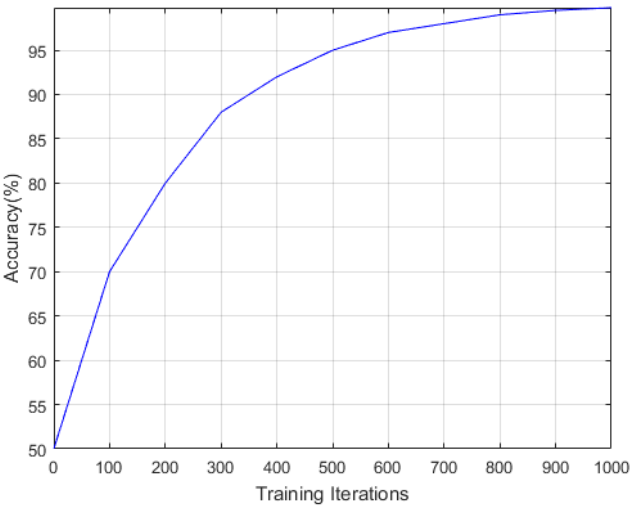

Figure 8. *Memory accuracy performance.*

Moreover, Figure 8 depicts the memory performance while Figure 9 shows the memory writing error, with both illustrations trained over 1000 iterations using the Wisconsin dataset. Incorporating this cell in a 9-10-2 AANN architecture for breast cancer diagnosis attains a memory erasing/reading accuracy of 99.8 % with 0.2 % writing error, indicating a high resolution with faster learning.

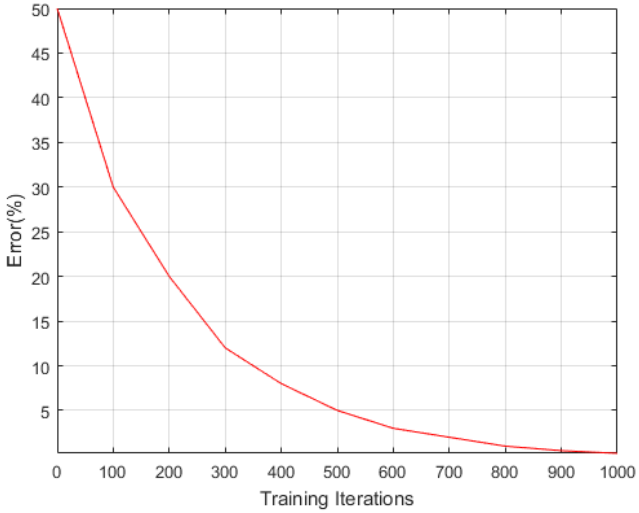

Figure 9. *Memory writing error.*

3.3. Memory Effectiveness

This section analyzes the cell effectiveness through the hysteresis loop characteristic and the total power consumption during operation, as depicted in Figure 10 to Figure 11. It recognizes the importance of energy efficiency for AANNs. Examining its effectiveness achieves a comprehensive understanding of the trade-offs and integration of this cell into energy-constrained neuromorphic systems.

The hysteresis characteristic of the memory cell is depicted in Figure 10. The drain current increases as V_{ds} increase from negative to positive in sweep-up, indicating that the memory is in its programming state. On the other hand, the drain current decreases as V_{ds} decrease from positive to negative, indicating that the memory is in its erasing state. It is observed that the sweep-up and sweep-down curves do not overlap, indicating hysteresis and forming a closed loop S-shaped with transistors operating in the subthreshold regime. The hysteresis loop indicates the memory's ability to retain its previous state to some extent after a voltage change. The hysteresis loop width, ΔV, indicates the memory can retain up to 2 V which is more than enough for AANN applications.

The memory cell's total power consumption is depicted in Figure 11. It is known that the total power consumption of a circuit is obtained by calculating the area under its graph. Thus, the memory cell’s power consumption is 1.06 µW under a typical operating voltage of 1 V. This power value is low compared to similar analog memory technologies.

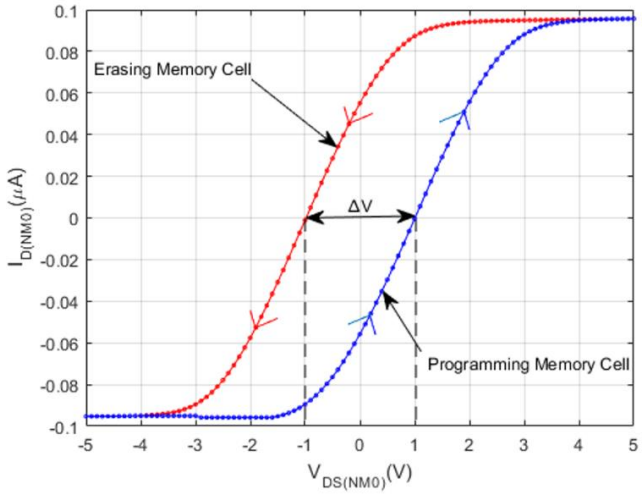

Figure 10. *Hysteresis sweep.*

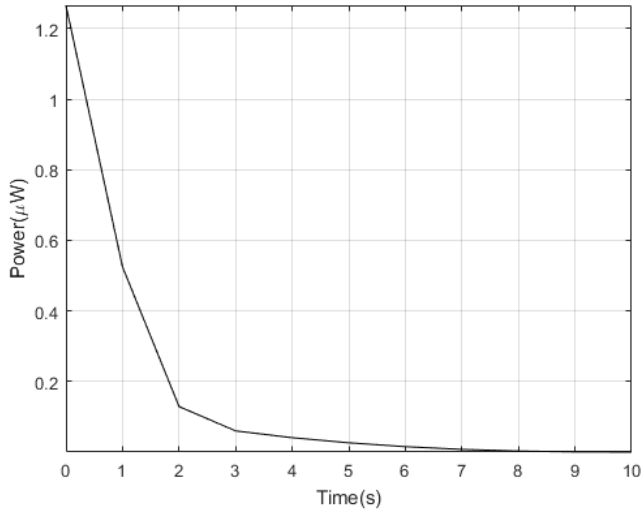

Figure 11. *Total power.*

4. Discussion

The results presented in the previous section reveal promising performance characteristics in storing and retrieving analog information reliably, providing a detailed understanding of the cell's operational characteristics and serving as a foundation for evaluating its suitability for applications in analog neural networks and other analog signal processing tasks. Moreover, this indicates that the injection rate remains nearly constant across a broad range of drain voltages. This phenomenon results from two opposing processes. Firstly, when the drain voltage exceeds the gate voltage, the electric field within the oxide layer hinders electron movement toward the gate, causing the injected electrons to return to the drain. Consequently, the injection efficiency diminishes as the drain voltage increases. Secondly, a rise in drain voltage enhances the electric field in the drain-to-channel depletion layer, significantly boosting the number of electrons with enough energy to overcome the 3.0 eV oxide potential barrier. Over a wide range of drain voltages, the reduction in efficiency is almost perfectly balanced by the growing number of hot electrons, resulting in a nearly constant injection rate. By setting the injection transistor drain voltage to 5 V for memory writing, the writing rate becomes stable despite minor variations in drain voltage.

Furthermore, the offset error could be influenced by the loop's time constant [19]. This offset primarily arises because the error signal in the negative feedback loop is the injection current, which is determined by the drain voltage of the injection transistor. However, the injection transistor's drain-to-gate capacitance, C_{dg}, creates an alternative positive feedback loop. This feedback loop introduces hysteretic responses, aiding the comparator in fully switching once it starts slewing in an unavoidable offset error at the cell output. Moreover, maintaining the memory cell precision relies heavily on power supply rejection [20]. The FG is referenced to the positive supply V_{dd} through transistor PM0, making the cell suitable for driving loads that are also referenced to V_{dd}. Ideally, the cell's output follows variations in V_{dd} with unity gain. The design parameters needed to achieve this unity gain from V_{dd} to V_{out} is obtained as follows:

First, by examining the feedback loop created by C_i, NM0, and PM0, with V_{dd} serving as the input and V_{out} as the output. Given an infinite loop gain, the resulting closed-loop transfer function is governed by equation (4).

$$G_\infty = \frac{V_{out}}{V_{dd}}\Big|_{T=\infty} = \frac{C_i+C_p}{C_i} = 1+\frac{C_p}{C_i} \tag{4}$$

Secondly, we wish to obtain a unity gain closed-loop transfer function from V_{dd} to V_{out}. This can be accomplished by setting a finite loop gain, T to offset α. The resulting closed-loop transfer function is given by equation (5).

$$\frac{V_{out}}{V_{dd}} = G_\infty \frac{T}{1+T} = \left(\frac{G_\infty}{1+\frac{1}{T}}\right) = \left(\frac{1+\alpha}{1+\frac{1}{T}}\right) \tag{5}$$

Choosing $\alpha = \frac{C_p}{C_i} = \frac{1}{T}$ gives $\frac{V_{out}}{V_{dd}} = 1$

The clear hysteresis loop observed in the I-V curves demonstrates the key memory effect of this device. The width of the loop suggests that the cell can reliably store analog values for a significant period, which is crucial for memory functionality. The results on programmability and resolution suggest that the cell can be precisely controlled to store a range of analog values. The good linear relationship between the injected charge and output voltage indicates effective programmability with resolution permitting the fine-tuning of the stored values. The retention characteristics demonstrate the memory cell's ability to maintain stored analog information over time with an encouraging observed decay rate. While noise tolerance and writing error are expected, the observed sensitivity suggests that the cell is within reliable tolerance operation in noisy environments with minute error, indicating that slide optimization is needed. The observed

total power consumption suggests that the device could be integrated into low-power systems.

Additionally, the results demonstrate that the analog FG transistor memory cell possesses promising characteristics for analog information storage and processing. This memory cell could be potentially integrated into more complex networks, for example, [21], for advanced analog signal processing in neuromorphic computing applications.

5. Conclusions

This work presented the design and characterization of a high-resolution non-volatile FG transistor memory cell suitable for on-chip learning in AANNs. The proposed cell utilizes a novel combination of advanced techniques, including hot-electron injection by introducing base implants and gate oxide tunneling to achieve high-density, non-volatile storage with exceptional analog characteristics. The results demonstrate the feasibility of the proposed cell as an efficient component for on-chip learning. The high-resolution analog storage capacity, low power consumption, and non-volatility of the cell offer significant advantages over conventional digital memory approaches, paving the way for efficient and scalable analog neuromorphic systems. The demonstrated memory characteristics offer the potential for implementing highly accurate analog synaptic weights within the AANNs, thereby enabling efficient and precise learning. The study highlights the significant potential of FG memory cells for enabling truly integrated, low-power, and high-performance on-chip learning systems. Future research will focus on further optimization of the cell design and integration into larger-scale AANN architectures for real-world applications. This work paves the way for developing sophisticated neuromorphic systems that mimic the human brain's computational capabilities and revolutionize artificial intelligence and machine learning research.

Abbreviations

AI	Artificial Intelligence
AANNs	Analog Artificial Neural Networks
FG	Floating Gate
CMOS	Complementary Metal-Oxide Semiconductor
MOSFET	Metal–Oxide Semiconductor Field-Effect Transistor

Author Contributions

Koagne Longpa Tamo Silas: Conceptualization, Investigation, Methodology, and Writing – original draft

Djimeli-Tsajio Alain Bernard: Supervision, Writing – review & editing

Fotsing Talla Bernard: Formal Analysis

Lienou Jean-Pierre: Visualization

Geh Wilson Ejuh: Project administration and Writing – review & editing

Funding

No funding is raised for this research.

Data Availability Statement

Not applicable.

Conflicts of Interest

The authors declare no conflicts of interest.

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Biography

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Geh Wilson Ejuh is a distinguished academic researcher in Electrical and Electronic Engineering. He earned a BSc in Physics-Chemistry in 2003, obtaining an MSc in Physics in 2006. In 2013, he obtained his Ph.D. in Physics option Materials Sciences from the Faculty of Science of the University of Yaoundé 1, Cameroon. In 2014, he was promoted to Lecturer, in 2019 to Associate Professor, and in 2023, he was promoted to Professor of Physics. He was posted as Head of Services for Teaching and Academic Activities in NAHPI in 2017 and 2021 as Head of Services for continuous training in NAHPI, University of Bamenda. Currently, he contributes his expertise at the University of Dschang, IUT-FV Bandjoun, Cameroon, within the General and Scientific Studies department, and at the National Higher Polytechnic Institute of the University of Bamenda, in the Department of Electrical and Electronic Engineering.

Research Field

Koagne Longpa Tamo Silas: Medical informatics, Artificial Intelligence, Electrical and Electronic Engineering, Analog Artificial Neural Networks, Embedded Systems

Djimeli-Tsajio Alain Bernard: Telecommunications Engineering, Computer and Network Engineering, Artificial Intelligence, Biomedical Informatics, Software Engineering

Fotsing Talla Bernard: Information Systems, Business Informatics, Software Engineering, Programming Languages, Computer Engineering

Lienou Jean-Pierre: Telecommunications Engineering, Computer Engineering, Software Engineering, Computer Communications (Networks), Artificial Intelligence

Geh Wilson Ejuh: Electrical and Electronics Engineering, Optoelectronics, Photonic, Thermodynamics Properties, Organic and Pharmaceutical molecules